

# QOQAE

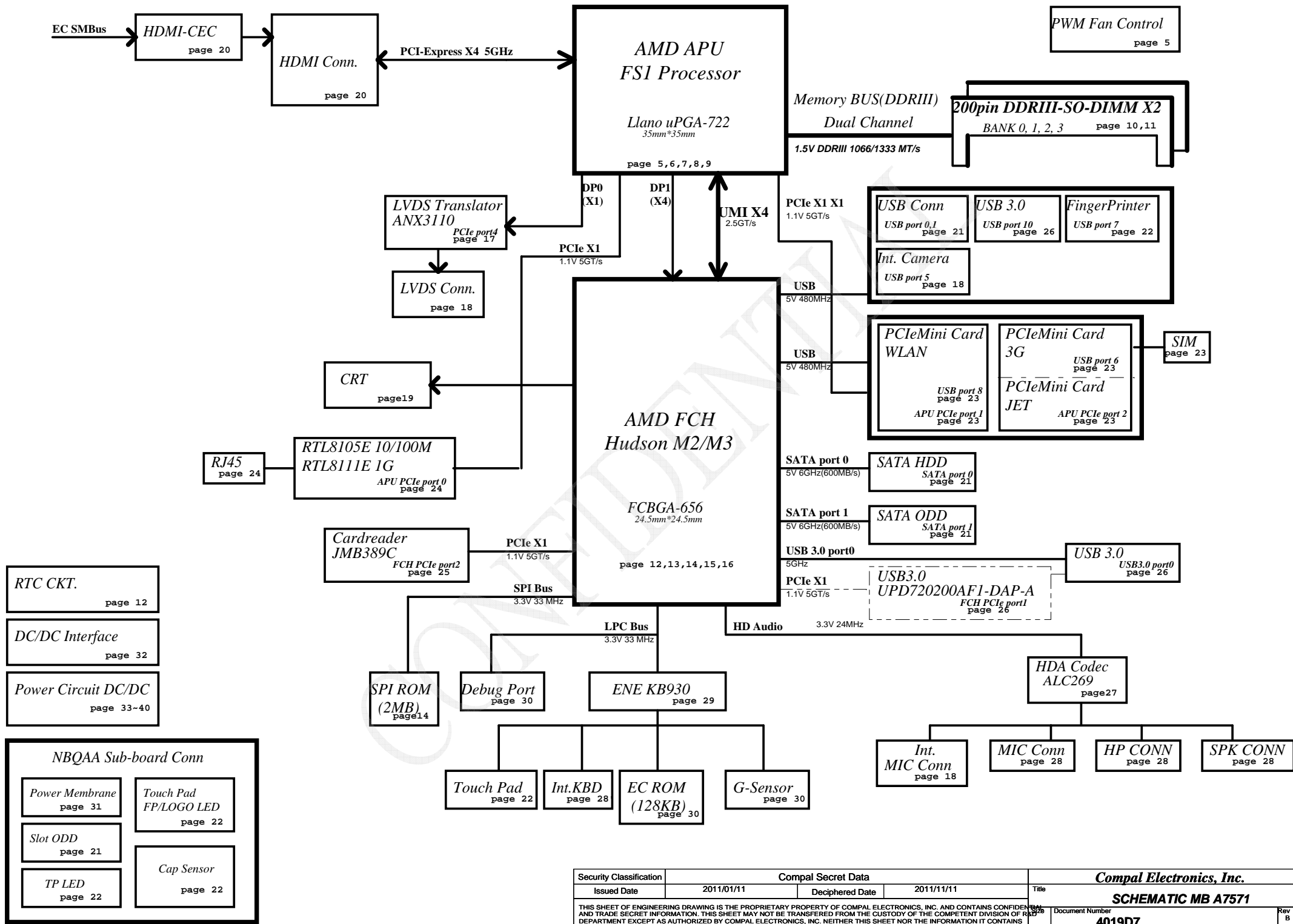
## Ontario 10AS

# LA-7571P REV 1.0 Schematic

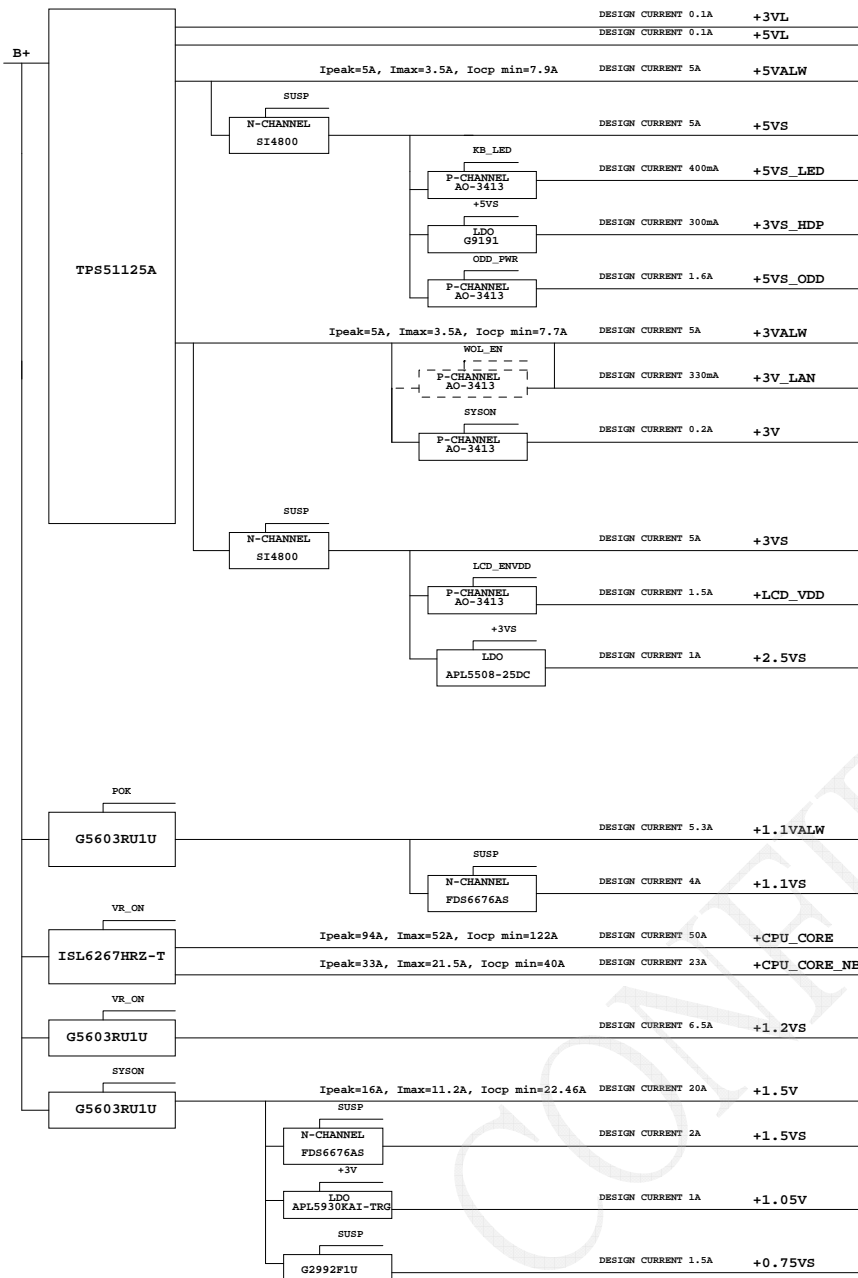
AMD Llano FS1 Processor / Hudson M2/M3

2011-05-04 Rev 1.0

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Voltage Rails

( O MEANS ON X MEANS OFF )

<div>power plane</div> <div>State</div>	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +1.1VALW +VSB	+1.5V +3V +1.05V	+5VS +3VS +2.5VS +1.5VS +1.2VS +1.1VS +0.75VS +CPU_CORE +CPU_CORE_NB
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

BTO Option Table

Function	HDMI-CEC		LAN		CAM+MIC	KB LED	Renesas USB3.0
description		Y	U	V	X	K	Reserved
explain	HDMI	HDMI+CEC	10/100	10/100/1000	CAM	KB LED	Renesas USB3.0
BTO		CEC@	8105E@	8111E@	CAM@	KBL@	RENE@

Function	ODD		Mini Card		Chipset		EC	
description		T	G	J	FCH		N/A	Reserved
explain	Normal	Slot	3G	JET	3G/JET		Hudson-M3	KB-930 KB-9012
BTO	ODD0@	ODD1@	3G@	JET@	3GJET@		HUDM3R1@ HUDM3R3@	KB930@ KB9012@

Function	FCH		UMA	
description	HM2	HM3	UM	
explain	Hudson-M2	Hudson-M3		
BTO	M2@	M3@		

STATE \ SIGNAL	SLP_S3#	SLP_S5#
Full ON	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH
S4 (Suspend to Disk)	LOW	HIGH
S5 (Soft OFF)	LOW	LOW
G3	LOW	LOW

FCH SM Bus Address (SCL0/SDA0)

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	WLAN		
+3VS	3G		

EC SM Bus1 Address

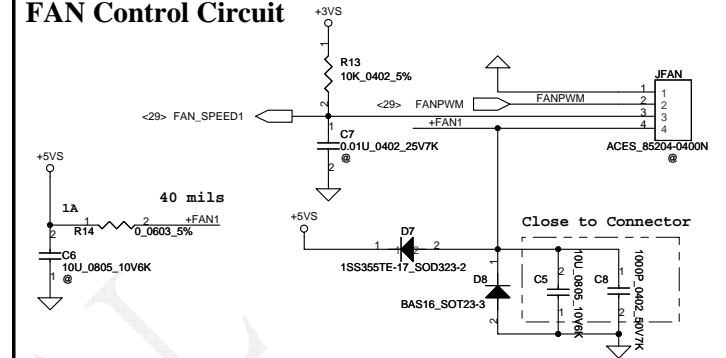
Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	HDMI-CEC	34 H	0011 0100 b
Power	Device	HEX	Address
+3VL	Cap. Sensor		Virtual I2C

EC SM Bus2 Address



Power	Device	HEX	Address
+3VS	G-Sensor	40 H	0100 0000 b





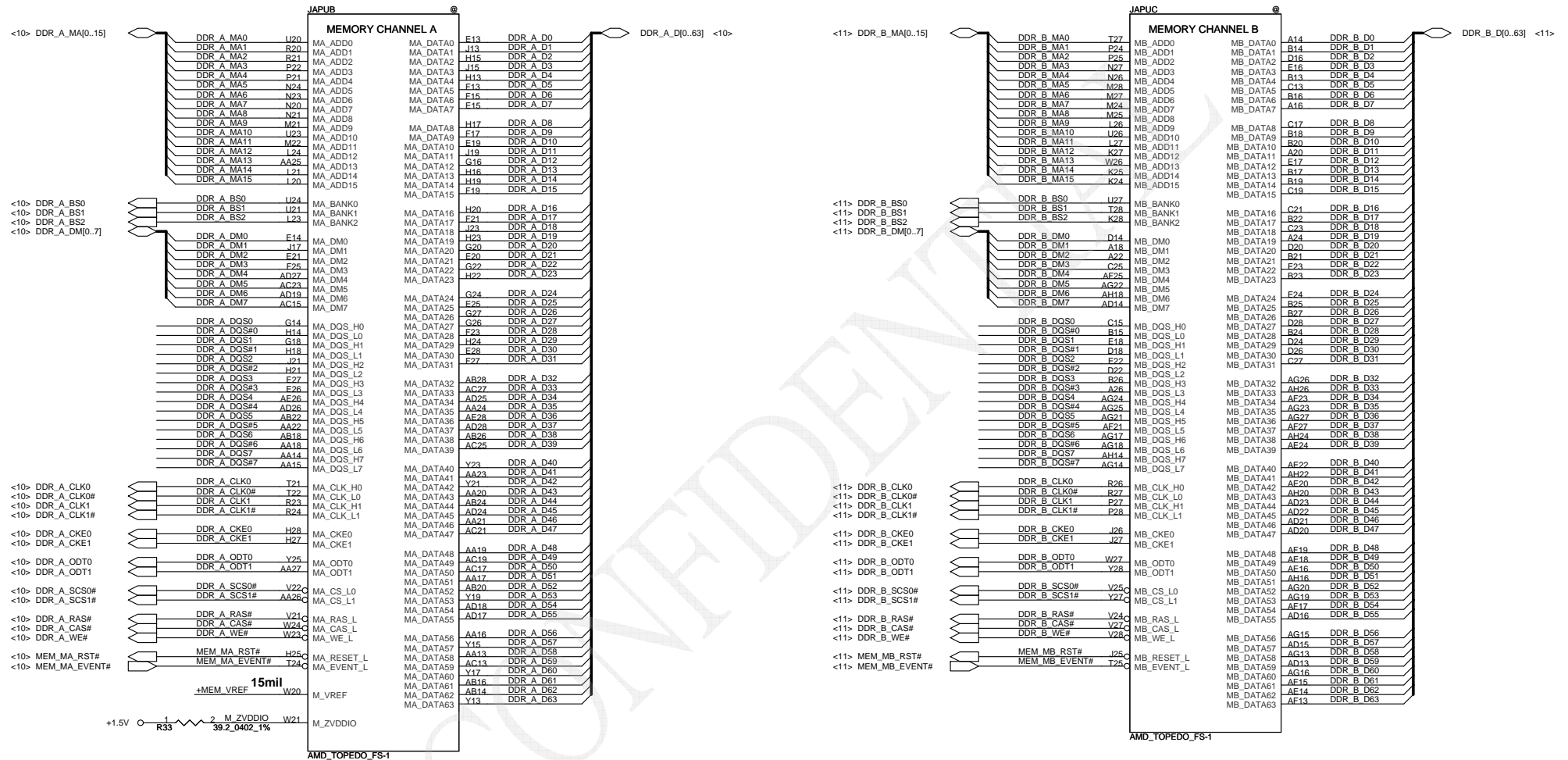
## FAN Control Circuit



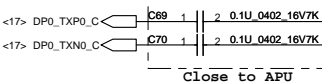
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<10> DDR\_A\_DQS[0..7]   
<10> DDR\_A\_DQS# [0..7] 

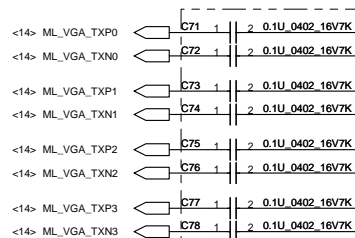
<11> DDR\_B\_DQS[0..7]   
<11> DDR\_B\_DQS# [0..7] 



# To LVDS Translator



## Close to APU



# To FCH

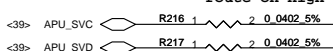
## 100MHz (SS)



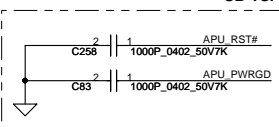
## 100MHz (NSS)



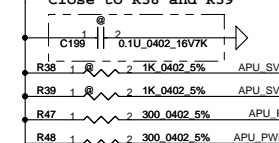
route on high speed layer



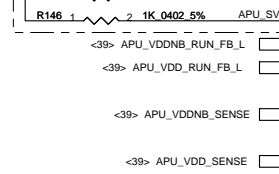
## SB-TSI



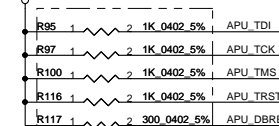
## Close to R38 and R39



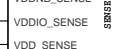
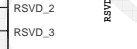
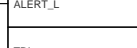
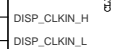
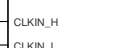
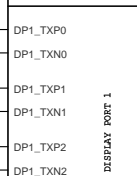
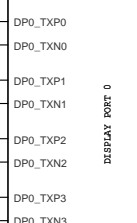
Avoid leakage issue



## Close to JHDT

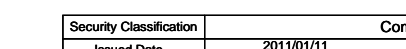
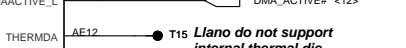
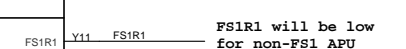
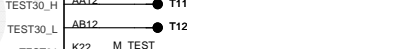
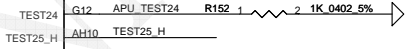
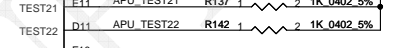
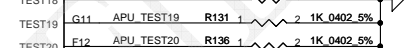
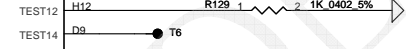
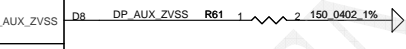
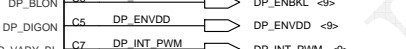
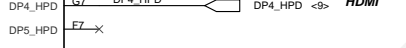
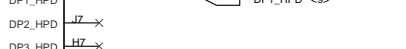
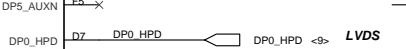
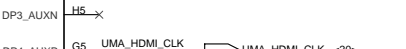
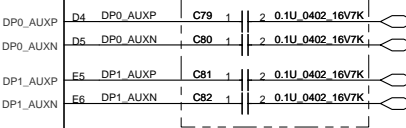


# APU



AMD\_TOPEDO\_FS-1

# Close to APU



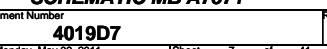
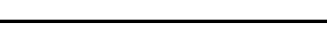
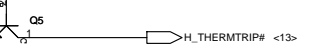
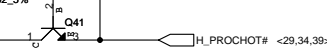
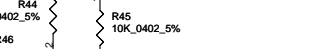
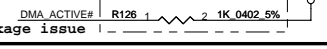
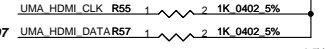
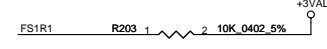
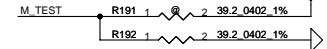
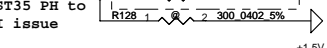
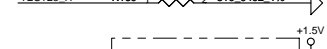
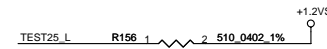
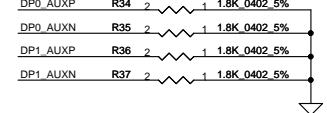
TEST4 THERMDA  
TEST5 THERMDC

# To LVDS Translator

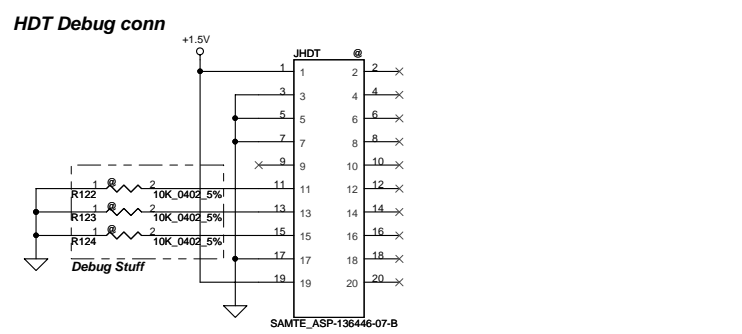
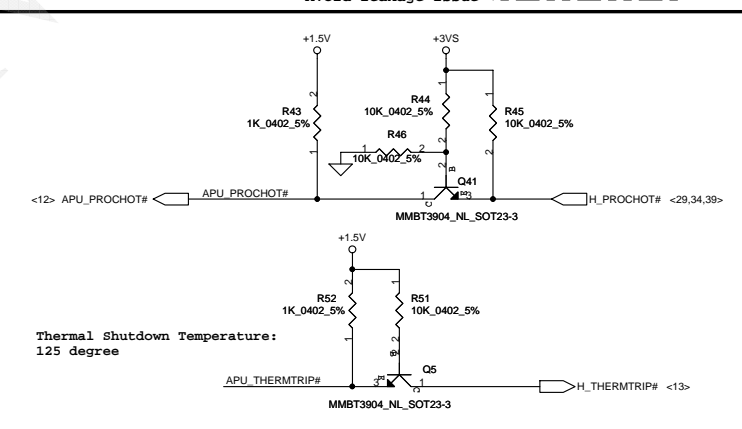
# To FCH

AUX 2~5 are for GFX interface use, they could be selected to DDC or AUX logic

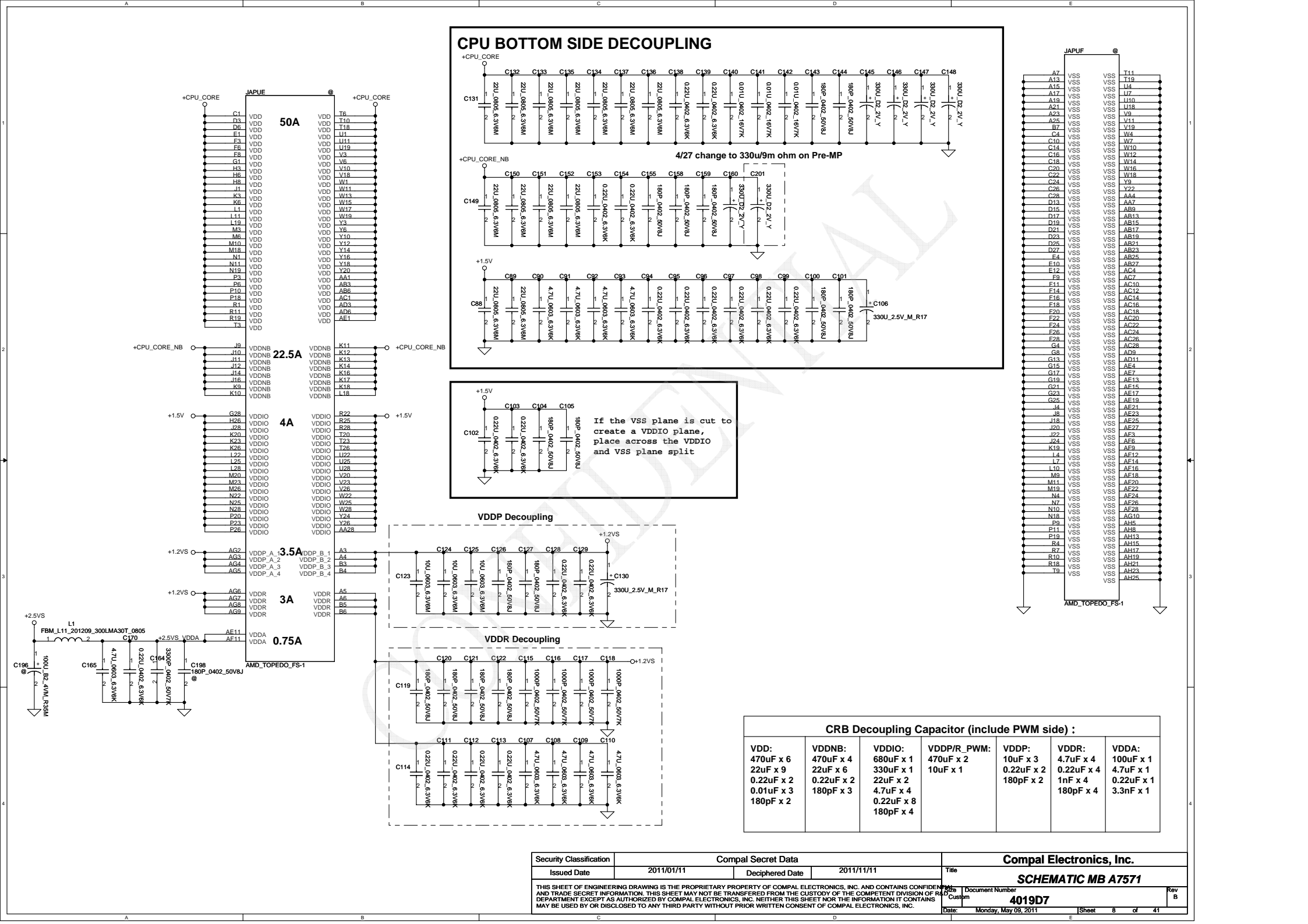
VDDIO level  
Need level shifter



TEST25 L  
TEST25 H  
TEST35  
M TEST  
FS1R1  
DMA ACTIVE#  
UMA HDMI CLK  
UMA HDMI DATAR57  
DMA ACTIVE#



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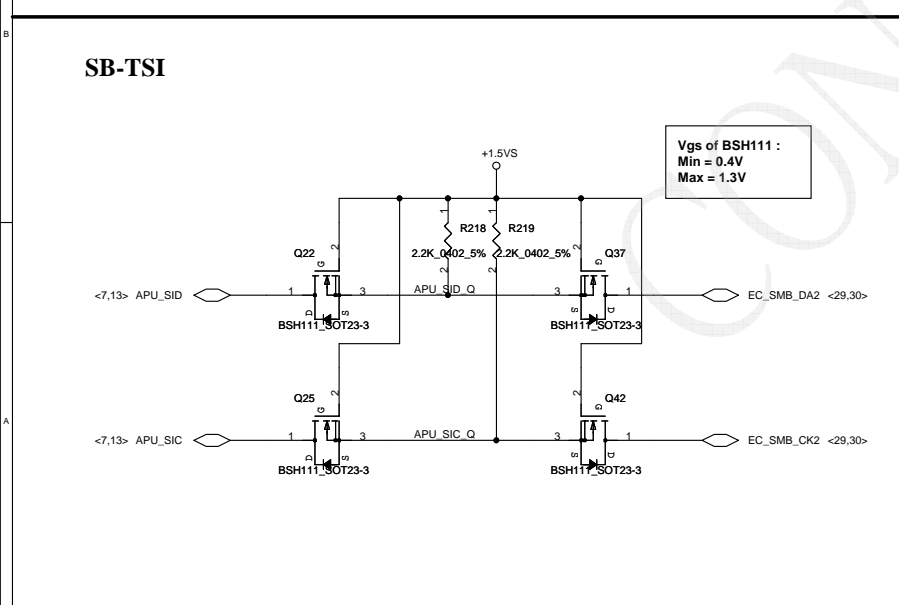
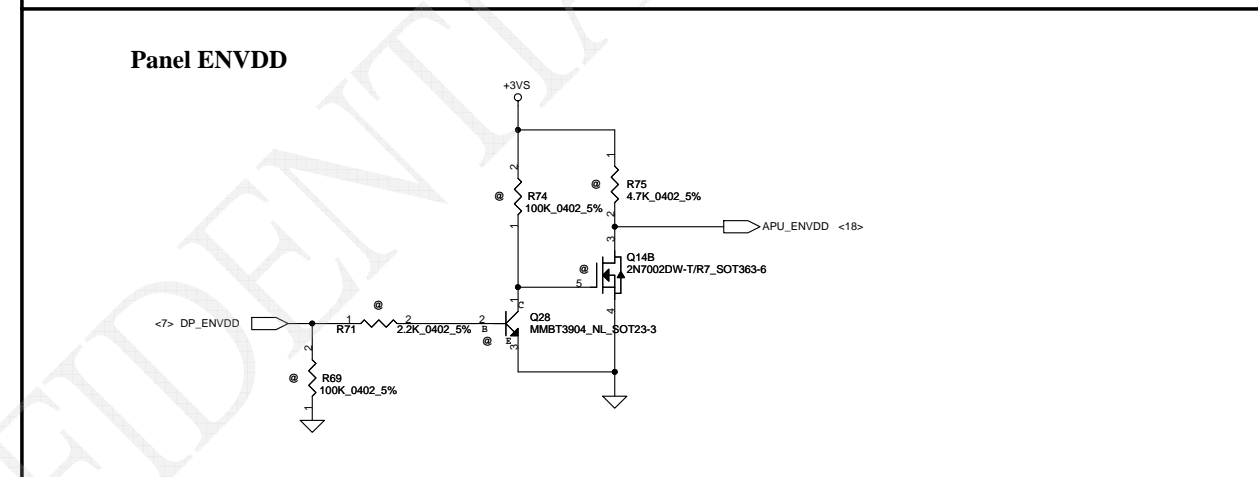
# HPD

The image displays three circuit diagrams for HPD (Hot Plug Detect) signals, each featuring a differential signal path and a pull-up network.

**Translator HPD**  
From Translator or Conn  
The input signal is **<17> LVDS\_HPD**. The circuit includes a pull-up network with resistors **R54** (10K\_0402\_5%) and **R59** (10K\_0402\_5%) connected to **+3VS**, and resistor **R60** (4.7K\_0402\_5%) connected to **+1.5VS**. The signal path passes through transistor **Q26** (MMBT3904\_NL\_SOT23-3) and is terminated by resistor **R207** (100K\_0402\_5%). The output is **DP0\_HPD <7>**.

**CRT HPD**  
From FCH  
The input signal is **<14> FCH\_CRT\_HPD**. The circuit includes a pull-up network with resistors **R150** (10K\_0402\_5%) and **R62** (10K\_0402\_5%) connected to **+3VS**, and resistor **R63** (4.7K\_0402\_5%) connected to **+1.5VS**. The signal path passes through transistor **Q16** (MMBT3904\_NL\_SOT23-3) and is terminated by resistor **R64** (100K\_0402\_5%). The output is **DP1\_HPD <7>**.

**HDMI HPD**  
From HDMI Conn  
The input signal is **<13,20> HDMI\_HPD**. The circuit includes a pull-up network with resistors **R267** (10K\_0402\_5%) and **R208** (10K\_0402\_5%) connected to **+3VS**, and resistor **R210** (4.7K\_0402\_5%) connected to **+1.5VS**. The signal path passes through transistor **Q27** (MMBT3904\_NL\_SOT23-3) and is terminated by resistor **R204** (100K\_0402\_5%). The output is **DP4\_HPD <7>**.

[illegible]

Need to confirm R93 value  
4.7K or 47K

<7> DP\_INT\_PWM

R89 2.2K\_0402\_5%

R76 4.7K\_0402\_5%

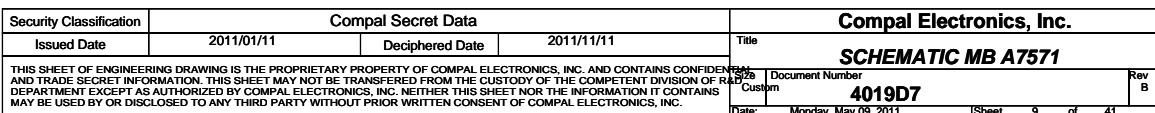
R92 47K\_0402\_5%

R93 47K\_0402\_5%

Q35 2N7002\_SOT23-3

Q21 MMBT3904\_NL\_SOT23-3

APU\_INV\_T\_PWM <17,18>



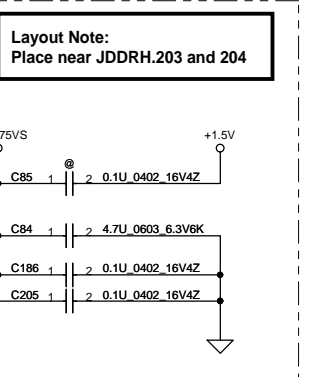
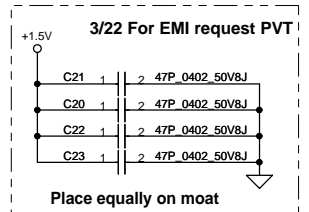
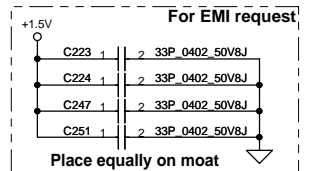
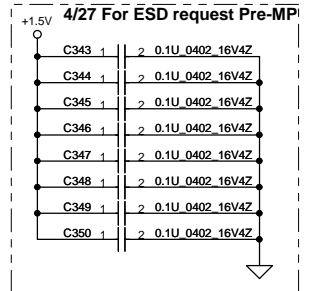
DDR\_A\_DQS[0..7] <6>

DDR\_A\_DQS# [0..7] <6>

DDR\_A\_D[0..63] <6>

DDR\_A\_MA[0..15] <6>

DDR\_A\_DM[0..7] <6>



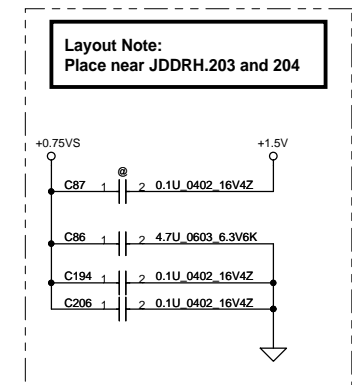
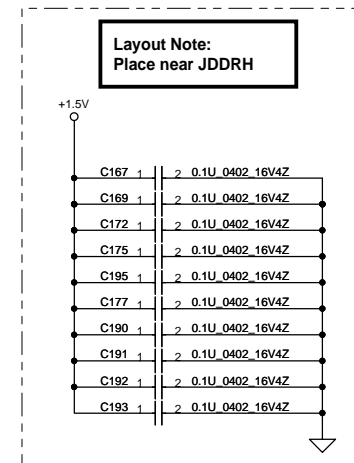
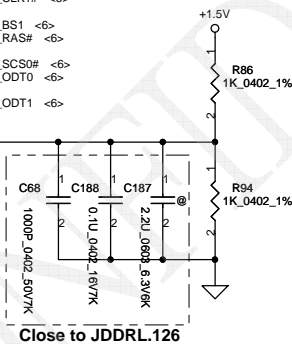
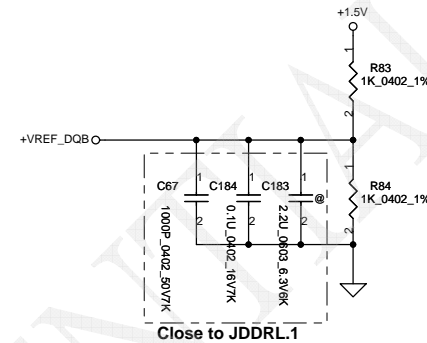
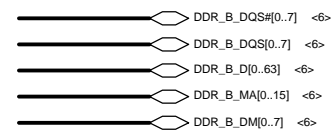
**SGA20331E10**  
330U\_D2\_2VM\_R8M

Part	Value
C218	1 2 0.1U 0402 16V4Z
C166	1 2 0.1U 0402 16V4Z
C168	1 2 0.1U 0402 16V4Z
C171	1 2 0.1U 0402 16V4Z
C174	1 2 0.1U 0402 16V4Z
C173	1 2 0.1U 0402 16V4Z
C176	1 2 0.1U 0402 16V4Z
C179	1 2 0.1U 0402 16V4Z
C178	1 2 0.1U 0402 16V4Z
C185	1 2 0.1U 0402 16V4Z
C180	1 2 0.1U 0402 16V4Z

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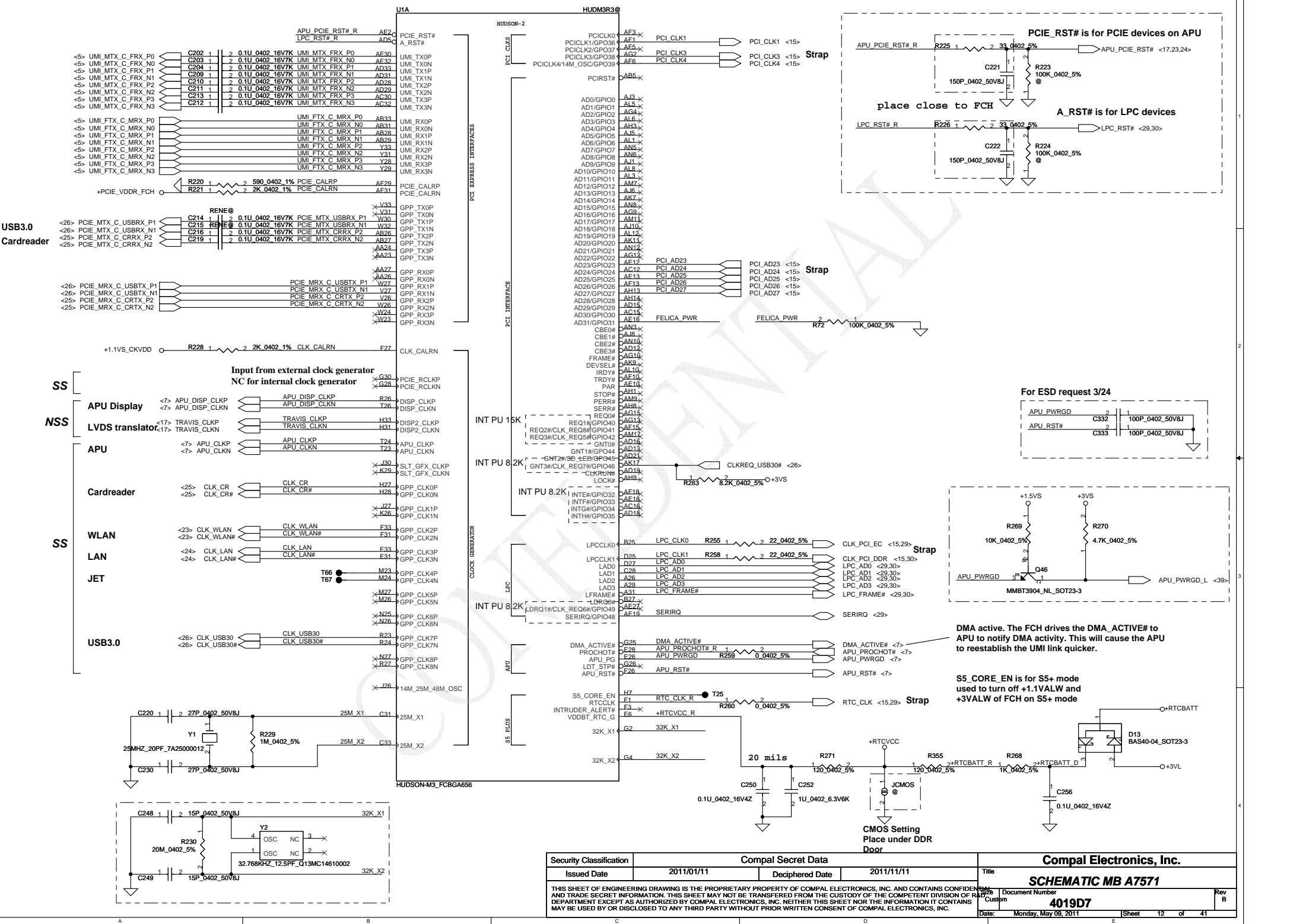
**Compal Electronics, Inc.**  
***SCHEMATIC MB A7571***

Part Number  
**4019D7**

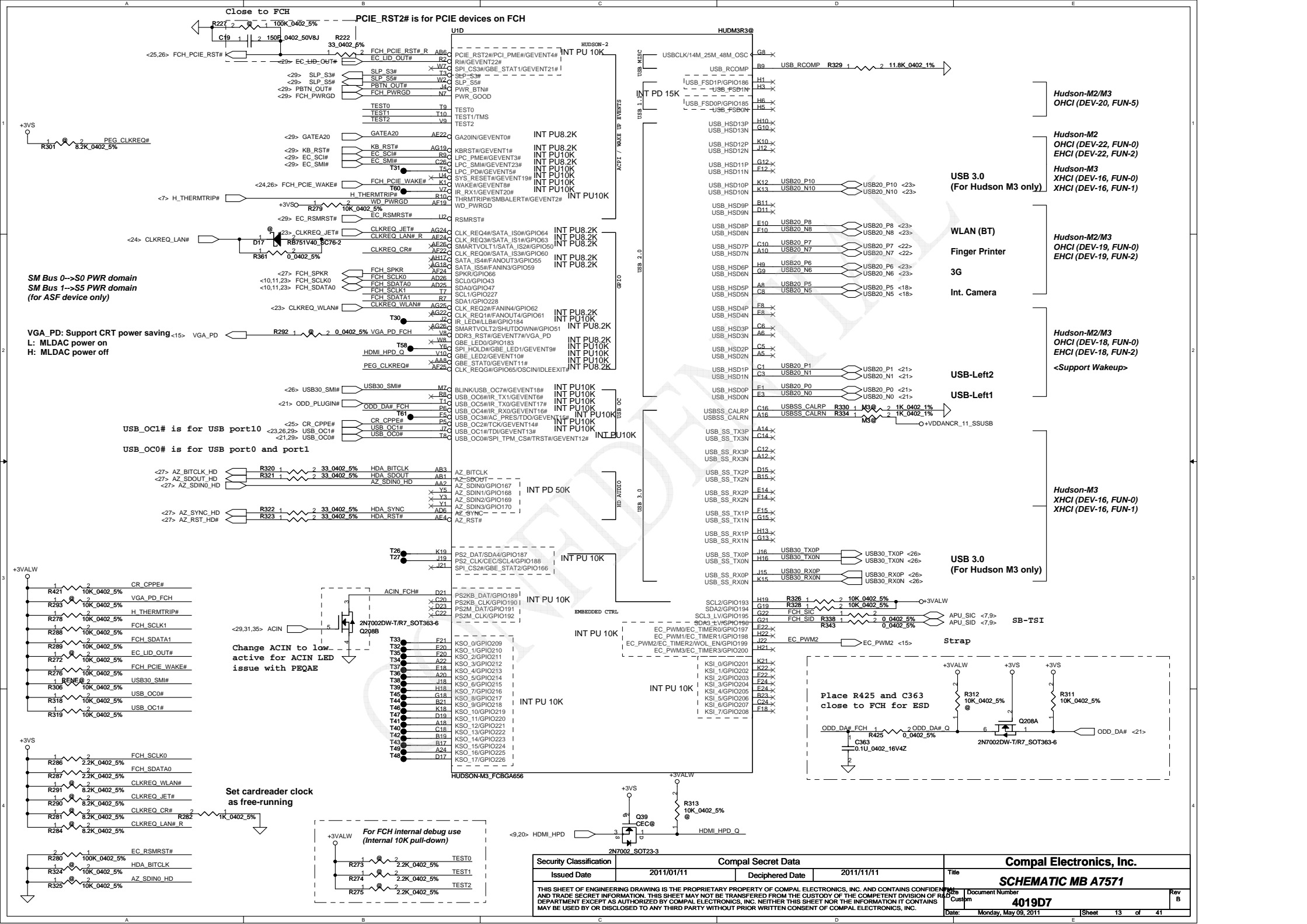


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Title			
<b>SCHEMATIC MB A7571</b>			
NT R&D	Size Custom	Document Number <b>4019D7</b>	Rev B
Date: Monday, May 09, 2011		Sheet 11 of 41	



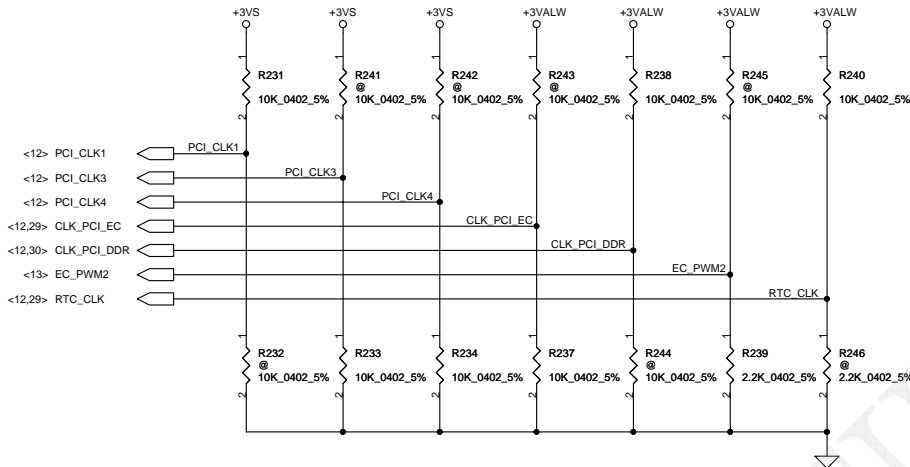
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								Rev A		Document Number		Rev B	
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## STRAP PINS

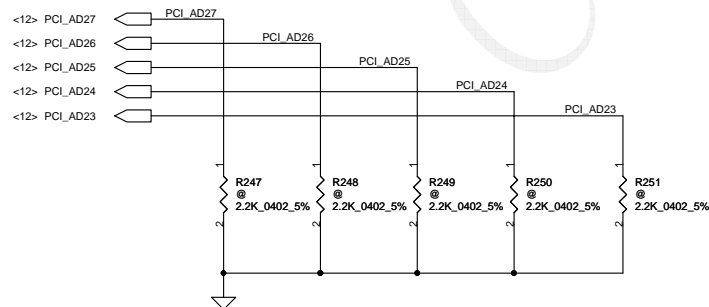
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	ENABLE DEBUG STRAP	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM (INTERNAL 10K PULL-UP)	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	DISABLE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



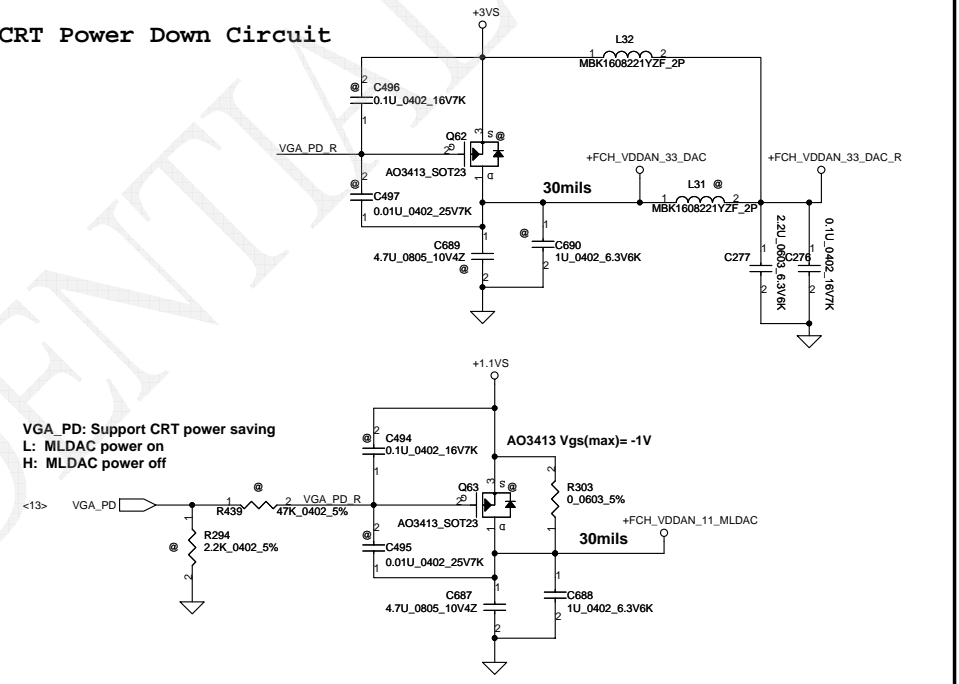
## DEBUG STRAPS

FCH HAS 15K INTERNAL PU-UP FOR PCI\_AD[27:23]

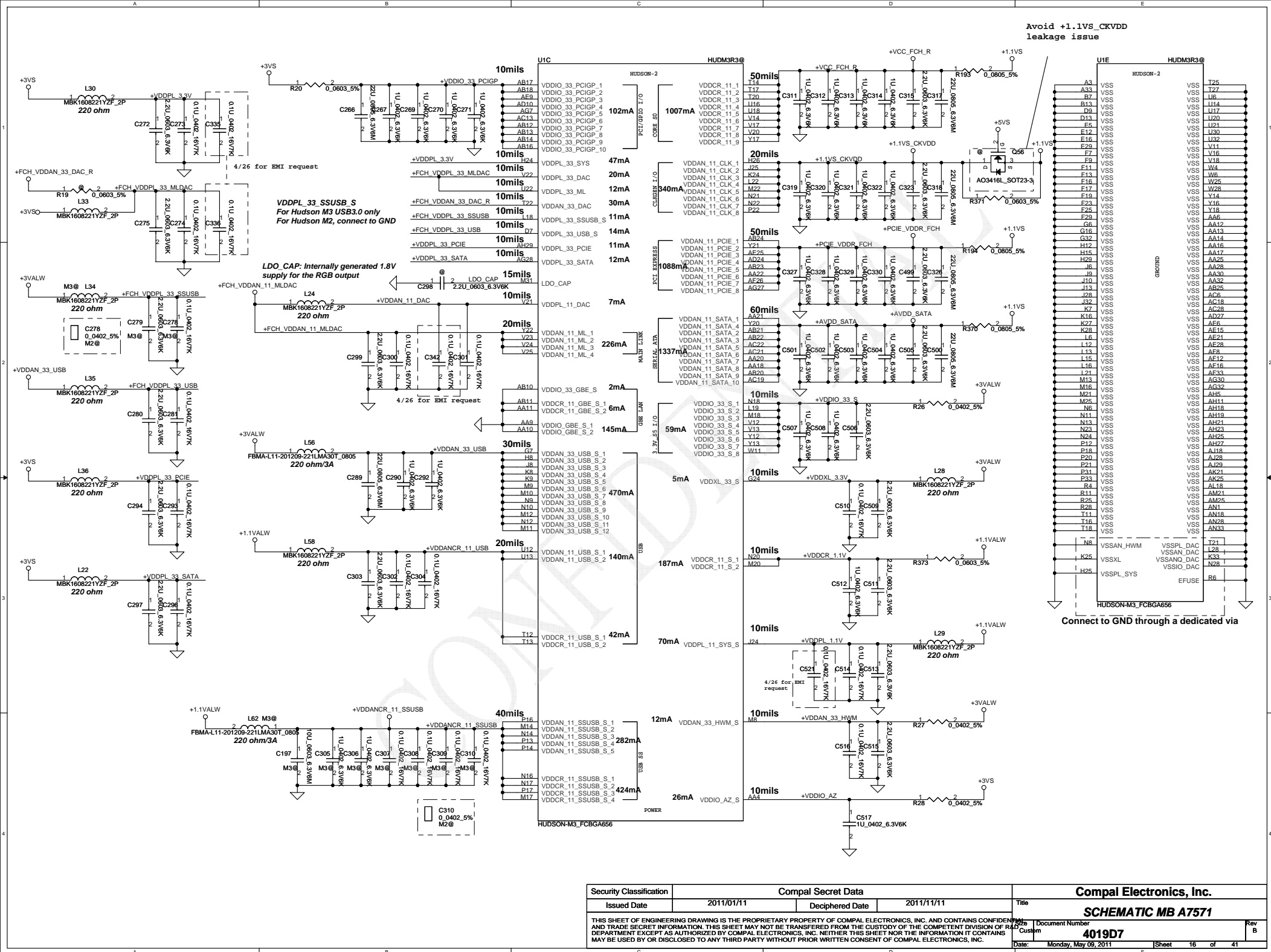
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



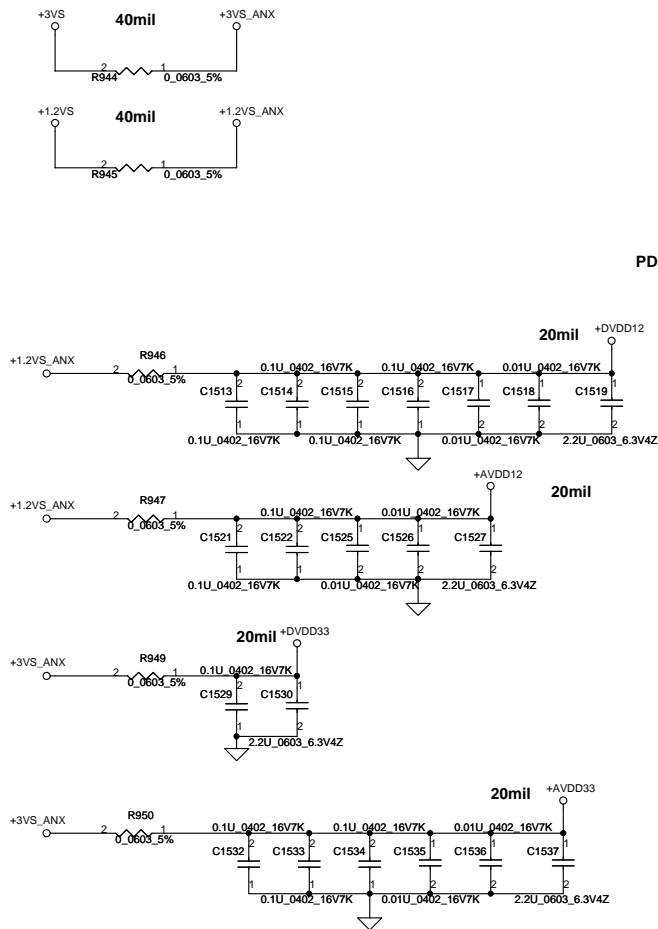
## CRT Power Down Circuit



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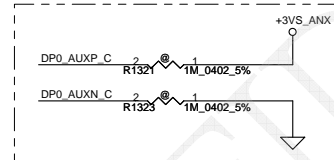




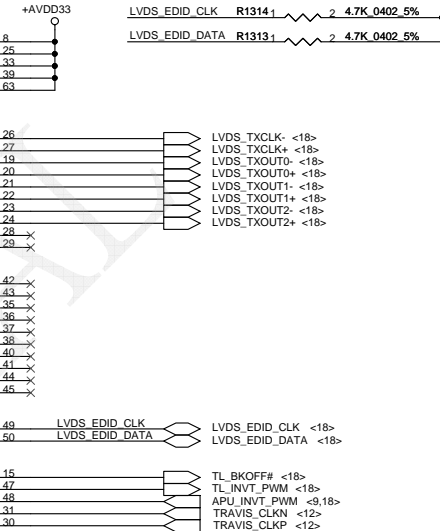
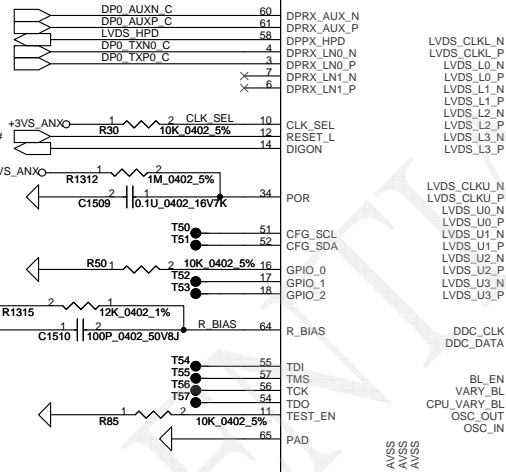
PD 100K at Page10

<7> DP0\_AUXN\_C  
<7> DP0\_AUXP\_C  
<8> LVDS\_HPD  
<7> DP0\_TXN0\_C  
<7> DP0\_TXP0\_C

<12,23,24> APU\_PCIE\_RST#  
<18> TL\_ENVDD

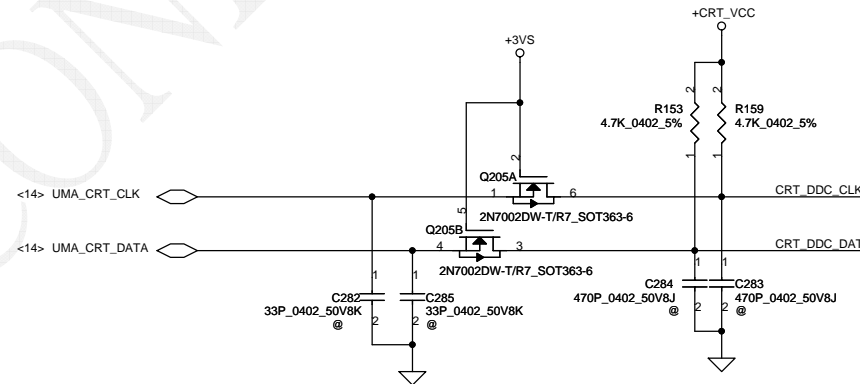
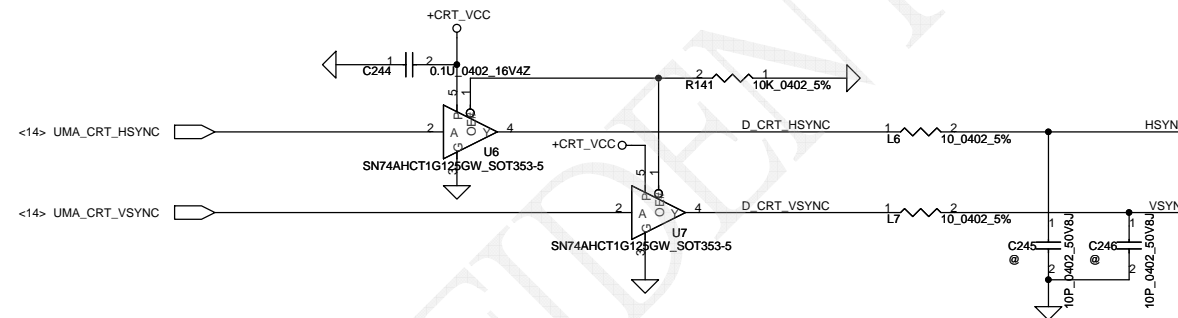
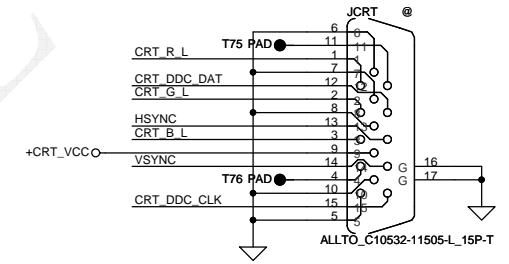
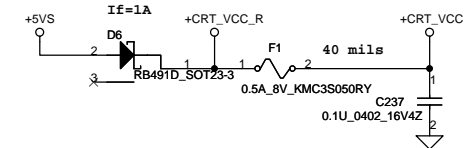
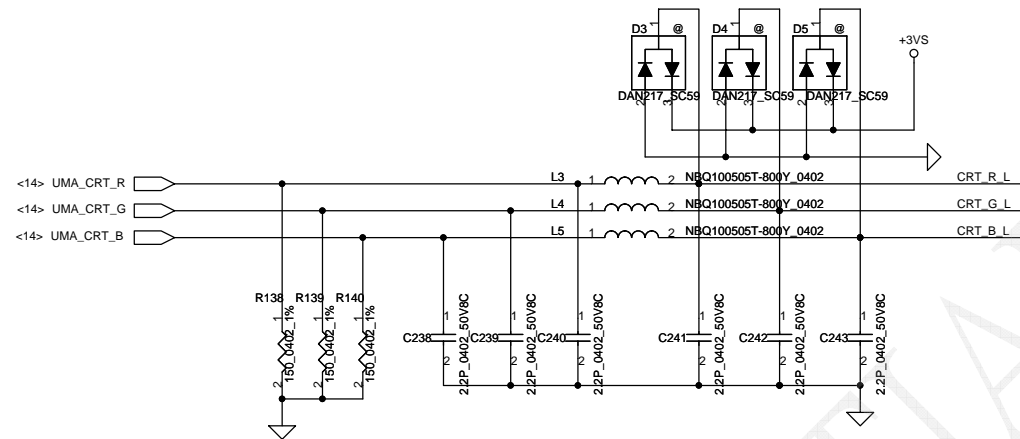


Place via on each trace bus and let resistor very close the via.

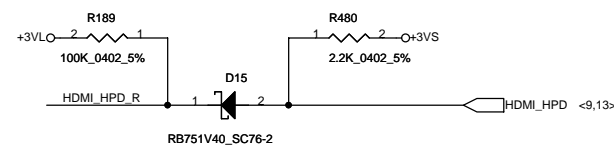
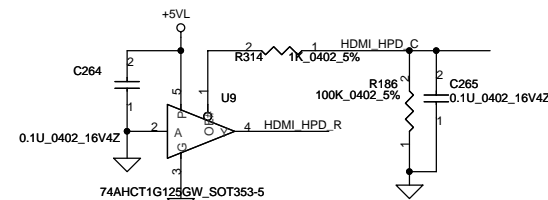
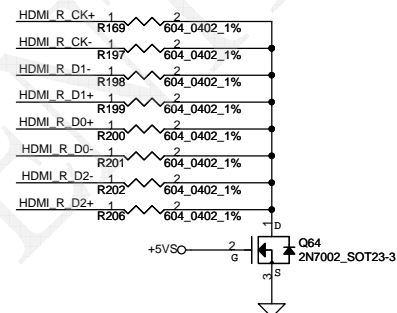
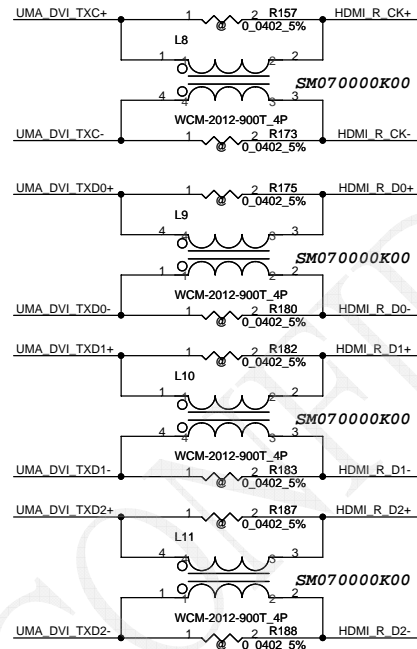
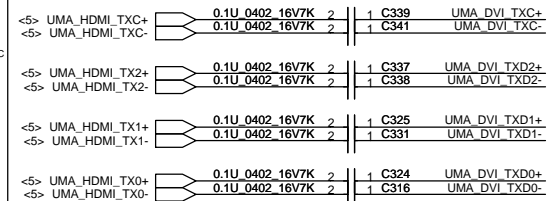


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				Date	Monday, May 09, 2011
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[illegible]

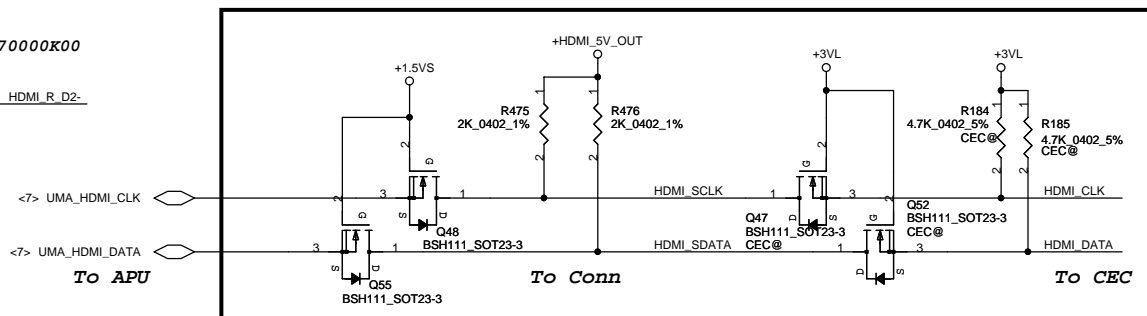
**JHDMI**

Pin	Signal
19	HPD_C
18	+HDMI_5V_OUT0
17	HDMI_SDATA
16	HDMI_SCLK
15	HDMI_CEC
14	HDMI_R_CK-
13	HDMI_R_CK+
12	HDMI_R_D0-
11	HDMI_R_D0+
10	HDMI_R_D1+
9	HDMI_R_D1-
8	HDMI_R_D2+
7	HDMI_R_D2-
6	D0_shield
5	D0+
4	D1+
3	D1-
2	D2+
1	D2-

HP\_DET  
+5V  
DDC/CEC\_GND  
SDA  
SCL  
Reserved  
CEC  
CK-  
CK\_shield  
CK+  
D0-  
D0\_shield  
D0+  
D1-  
D1\_shield  
D1+  
D2-  
D2\_shield  
D2+

GND 20  
GND 21  
GND 22  
GND 23

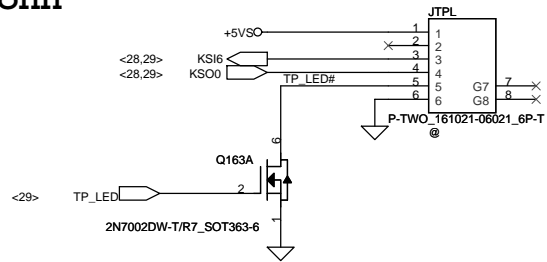
① TYCO 1939864-1 19P



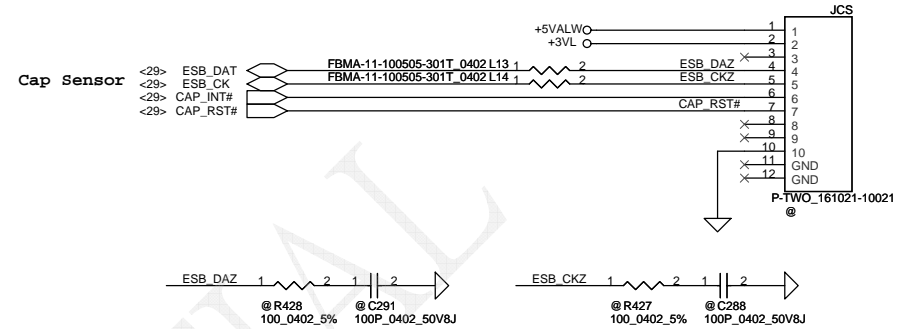
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				Date:	Monday, May 09, 2011	Sheet 20 of 41



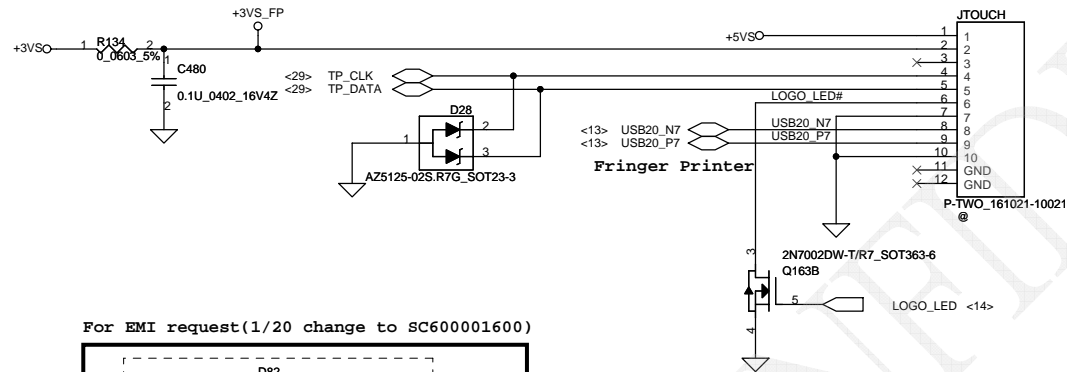
## TP LED Conn



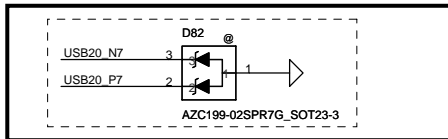
Cap Sensor Conn



## TP/B LED/B FP/B Conn

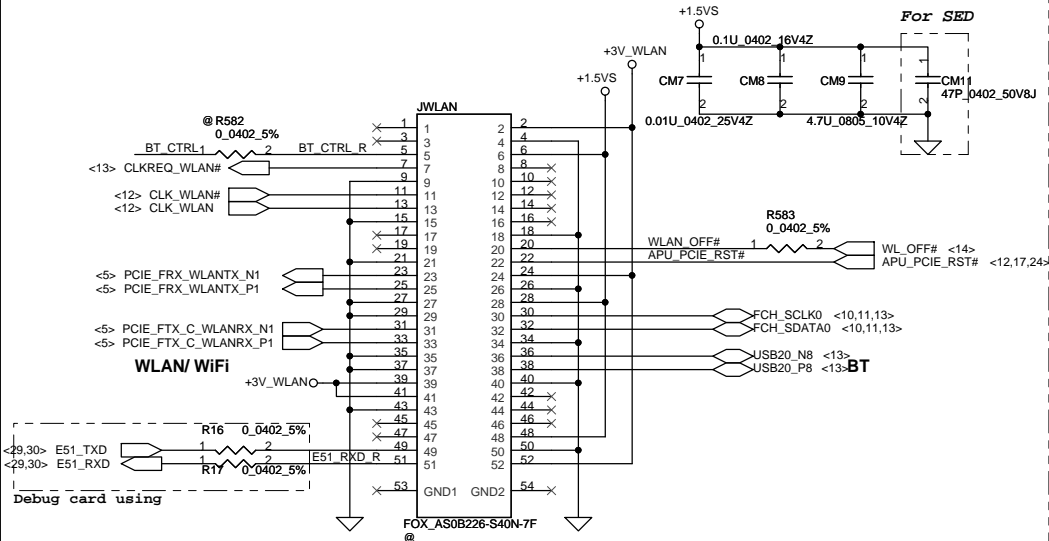
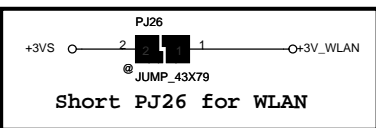


For EMI request(1/20 change to SC600001600)

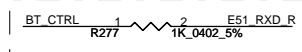


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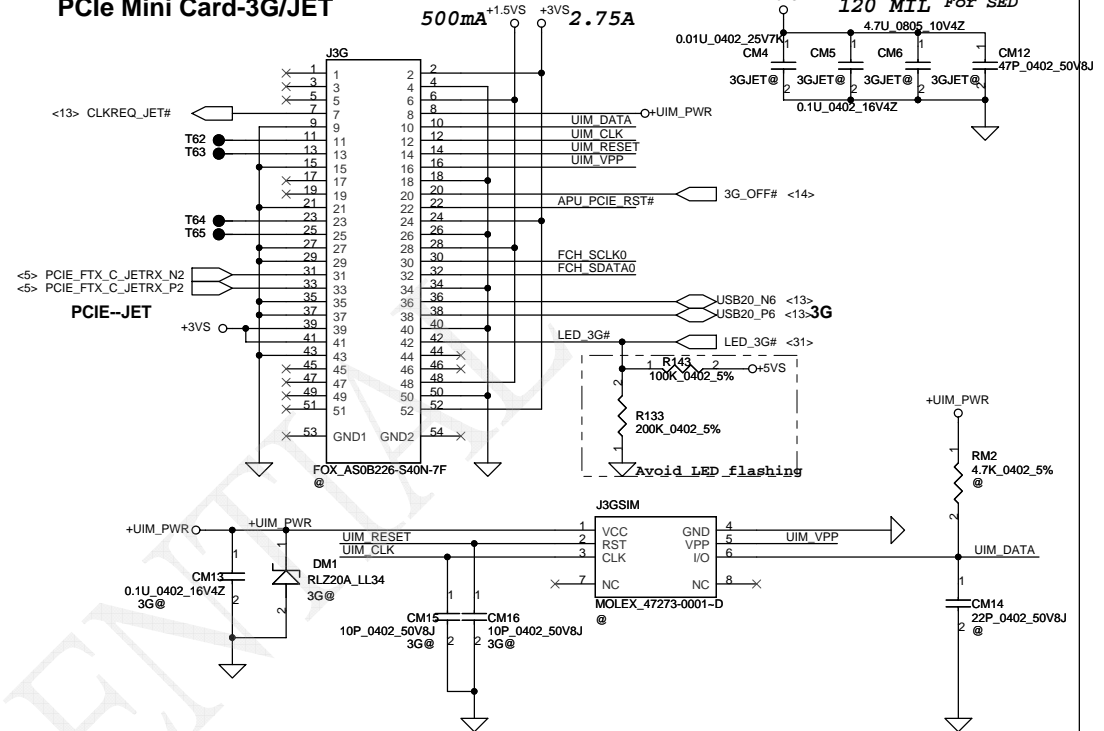
## PCIe Mini Card-WLAN



For Isolate Intel Rainbow Peak and Compal debug card

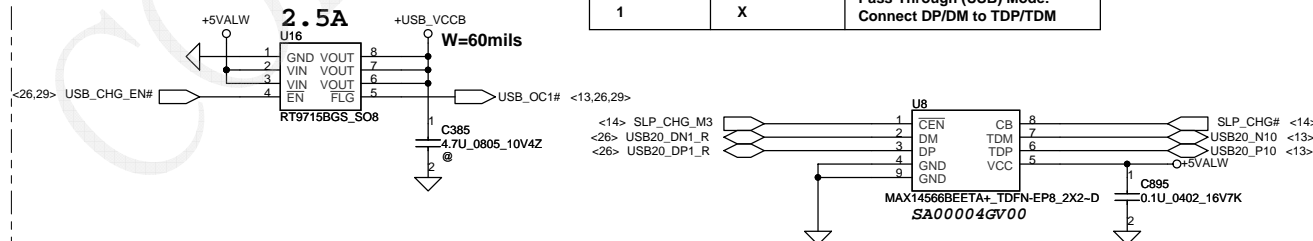


## PCIe Mini Card-3G/JET



## USB Sleep & Charge Auto-Mode Mode3/Mode4

MAX14566B		
CB SLP_CHG_M4	CB1 (CEN#) SLP_CHG_M3	STATUS
0	0	AUTO MODE (Including Mode 4)
0	1	Force Dedicated charger mode (MODE3)
1	X	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM



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				Size
				Document Number
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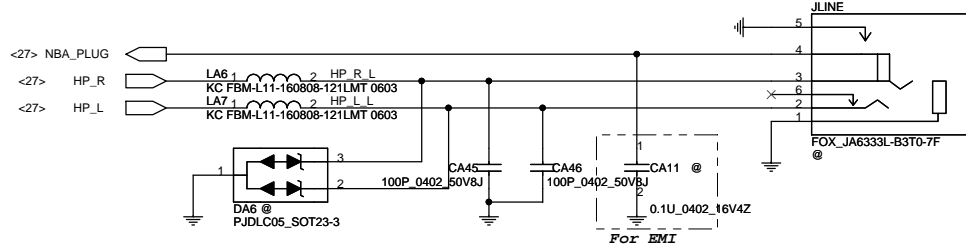




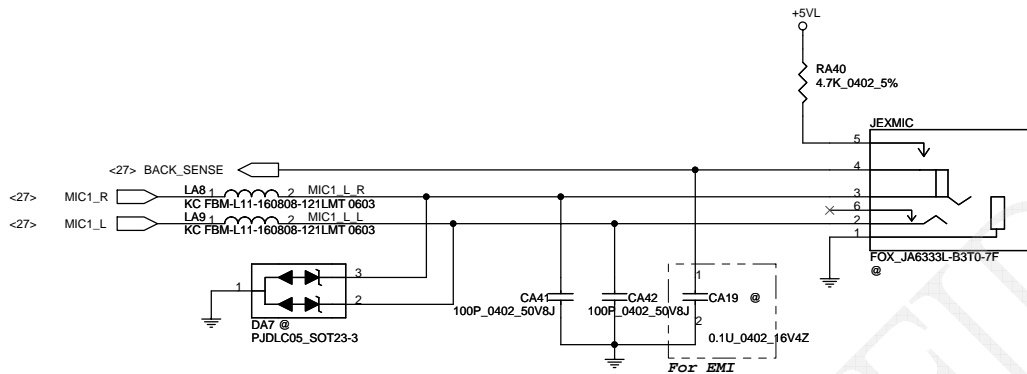




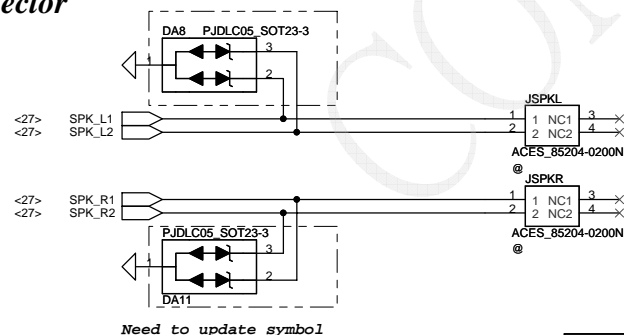
## HeadPhone/LINE Out JACK



## Ext.MIC/LINE IN JACK

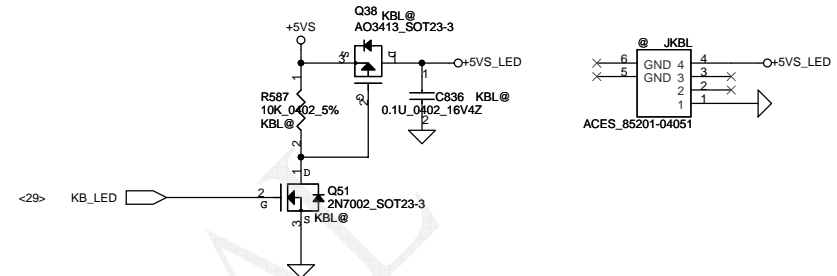


## Speaker Connector



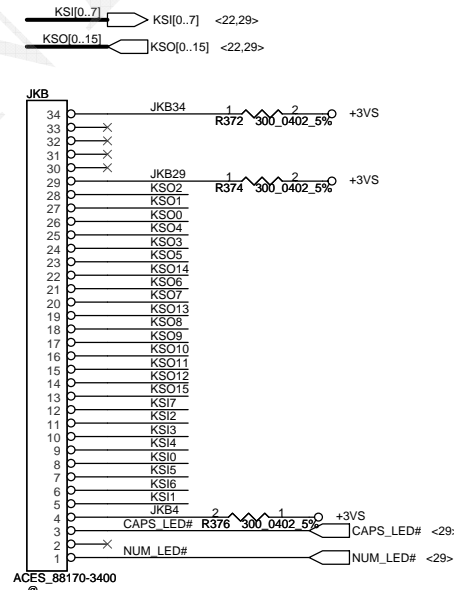
Need to update symbol

## Keyboard LED



## KEYBOARD CONN.

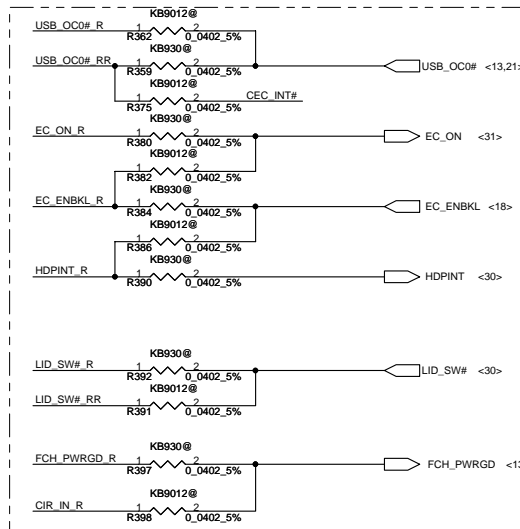
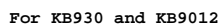
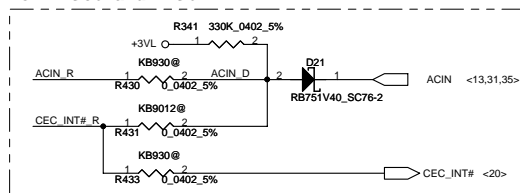
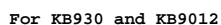
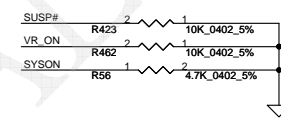
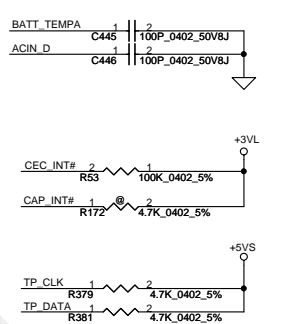
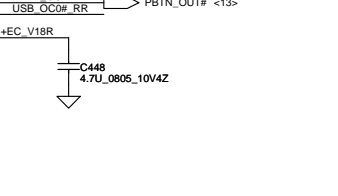
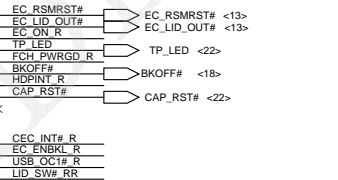
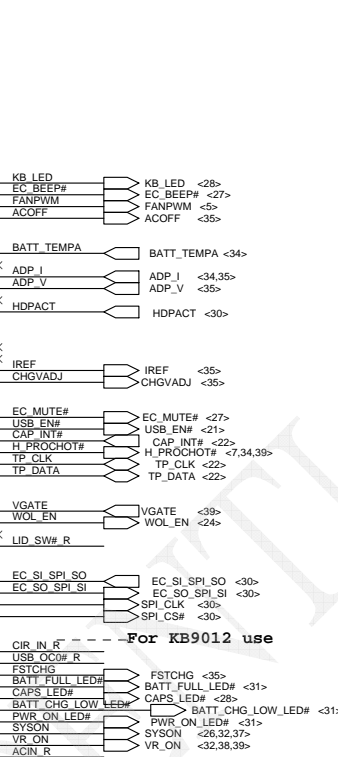
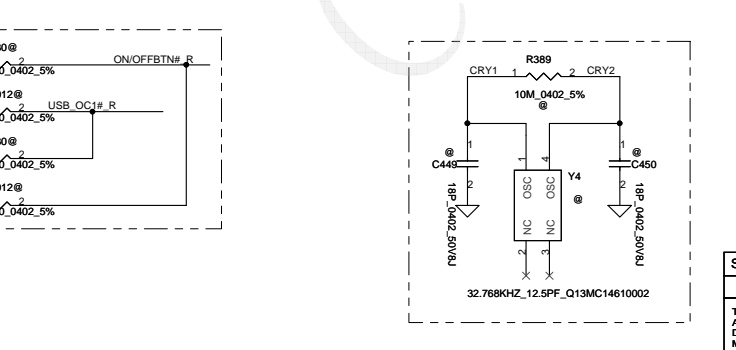
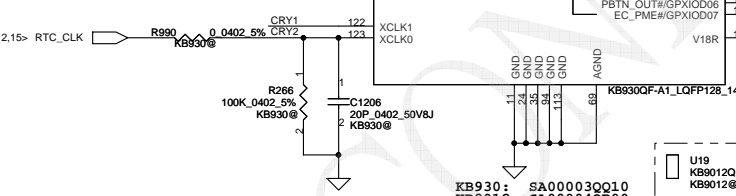
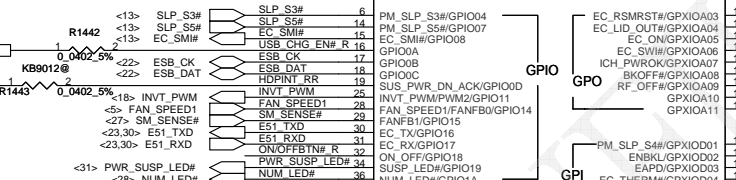
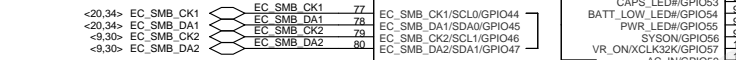
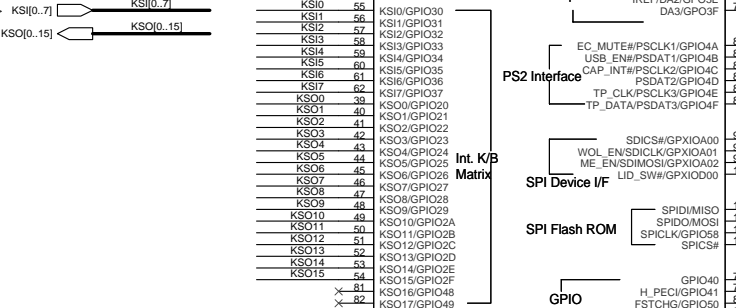
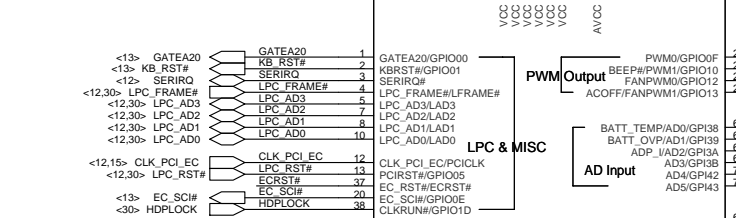
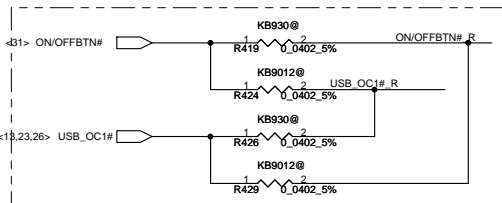
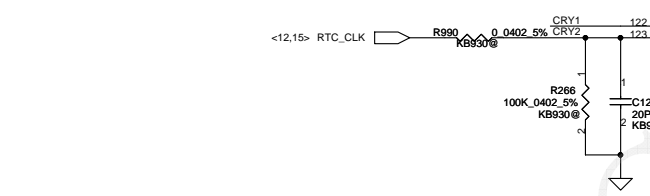
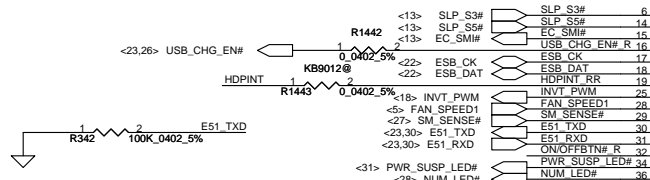
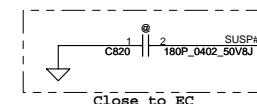
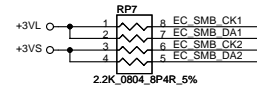
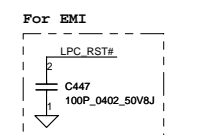
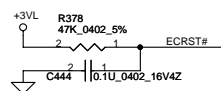
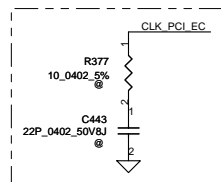
Notice: KB Connector Pin Definition Reversed with KB Membrane Pin Definition



please close to JKB

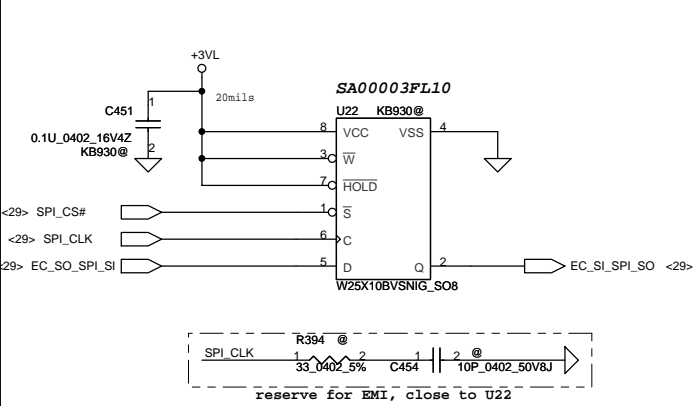
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KSO1	C405	1	2	100P_0402_50V8J
KSO0	C406	1	2	100P_0402_50V8J
KSO4	C407	1	2	100P_0402_50V8J
KSO3	C408	1	2	100P_0402_50V8J
KSO5	C409	1	2	100P_0402_50V8J
KSO14	C410	1	2	100P_0402_50V8J
KSO6	C411	1	2	100P_0402_50V8J
KSO7	C412	1	2	100P_0402_50V8J
KSO13	C413	1	2	100P_0402_50V8J
KSO8	C415	1	2	100P_0402_50V8J
KSO9	C416	1	2	100P_0402_50V8J
KSO10	C417	1	2	100P_0402_50V8J
KSO11	C418	1	2	100P_0402_50V8J
KSO12	C419	1	2	100P_0402_50V8J
KSO15	C420	1	2	100P_0402_50V8J
KSI7	C421	1	2	100P_0402_50V8J
KSI2	C422	1	2	100P_0402_50V8J
KSI3	C423	1	2	100P_0402_50V8J
KSI4	C424	1	2	100P_0402_50V8J
KSI0	C425	1	2	100P_0402_50V8J
KSI5	C427	1	2	100P_0402_50V8J
KSI6	C429	1	2	100P_0402_50V8J
KSI1	C431	1	2	100P_0402_50V8J
CAPS_LED#	C433	1	2	100P_0402_50V8J
NUM_LED#	C435	1	2	100P_0402_50V8J

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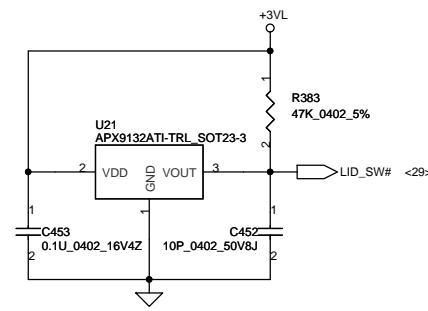


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				Document Number	<b>4019D7</b>

SPI Flash (128KB)

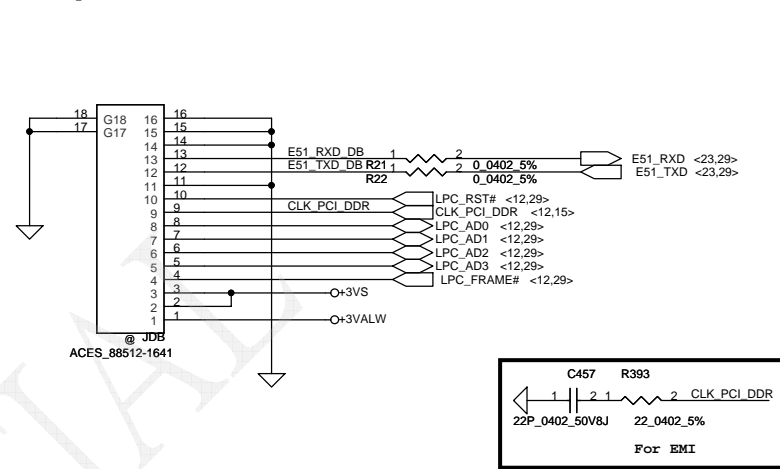


Lid SW

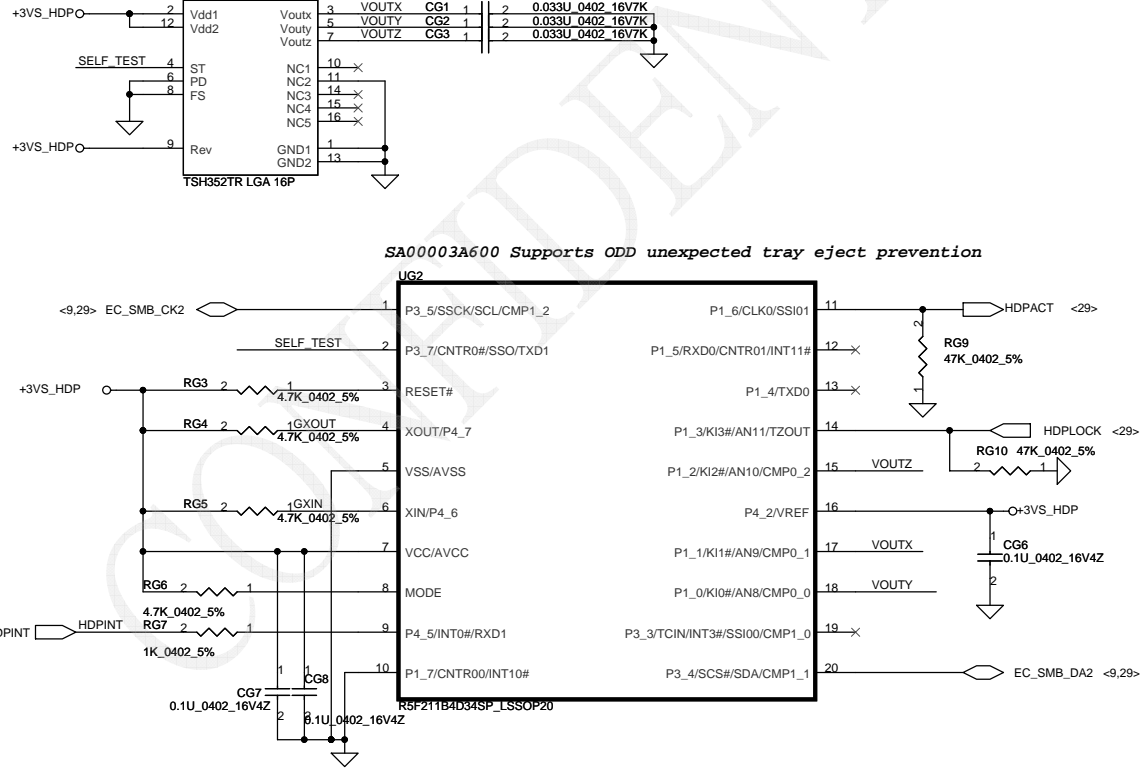
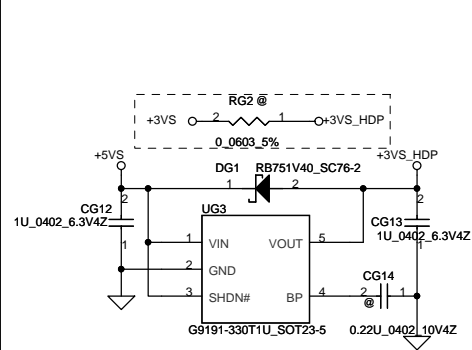


LPC / UART Debug Port

Please place JDB under DDR DIMM.

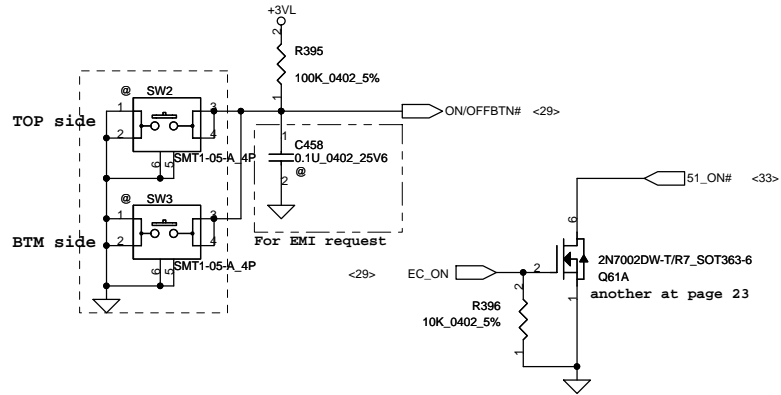


G-Sensor

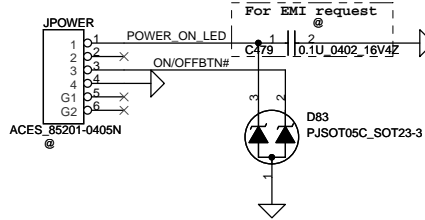


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4019D7				Rev B
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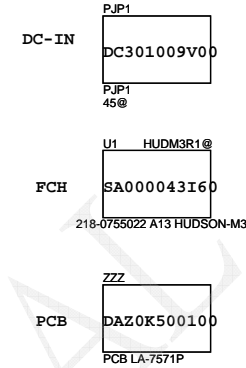
## Power Button



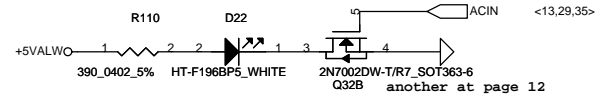
## PWR/B Conn



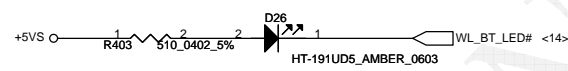
## ISPD



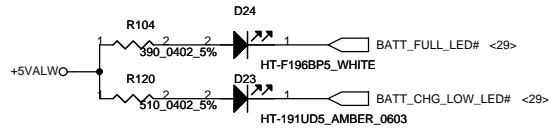
## DC-IN LED



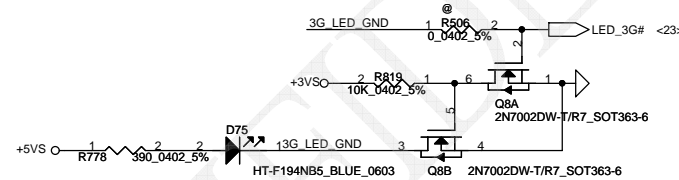
## WL/BT LED



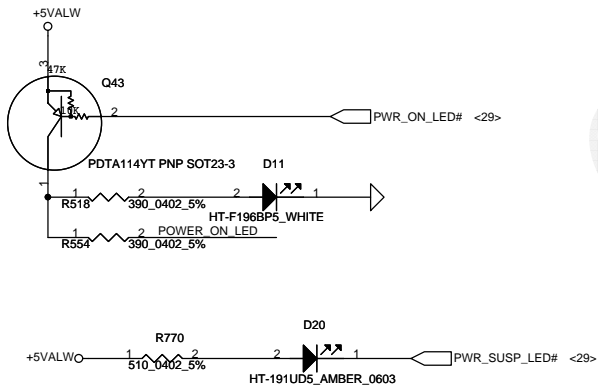
## BATT CHARGE/FULL LED



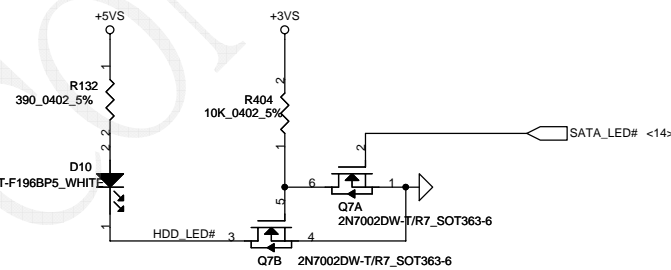
## WiMAX/3G LED



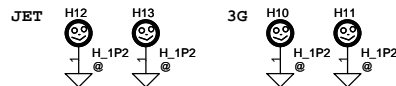
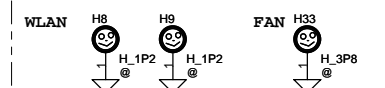
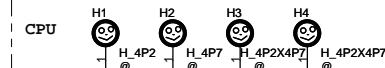
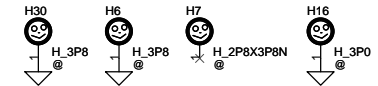
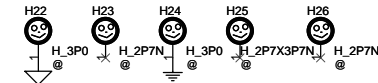
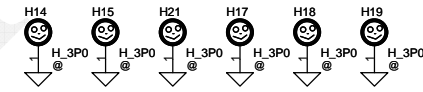
## POWER/SUSPEND LED



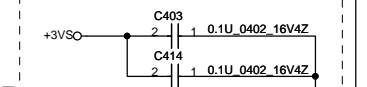
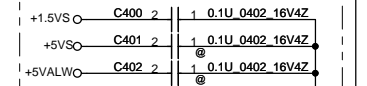
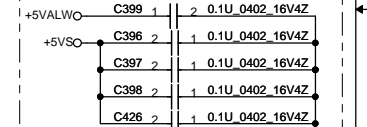
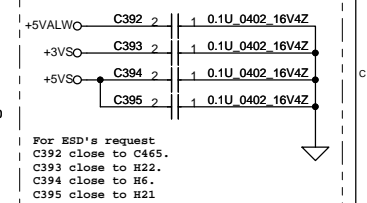
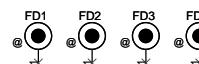
## HDD LED



## Screw Hole

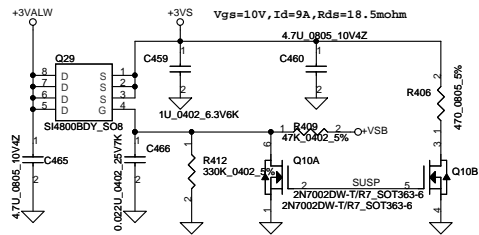


## PCB Federal Mark PAD

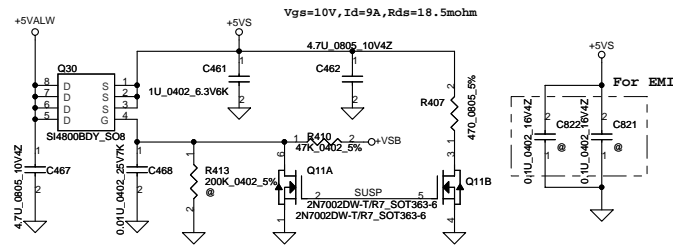


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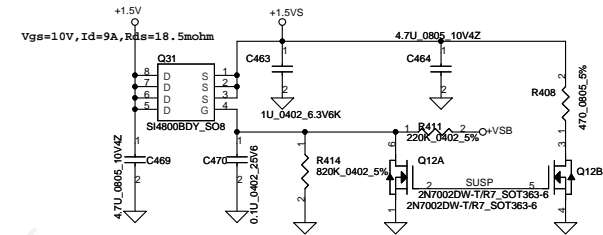
### +3VALW TO +3VS



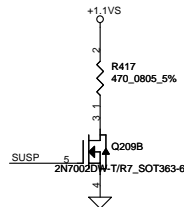
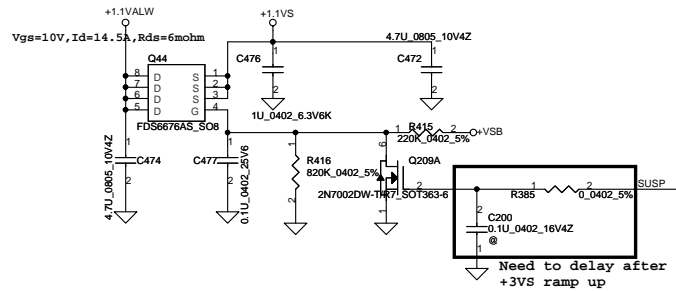
### +5VALW TO +5VS



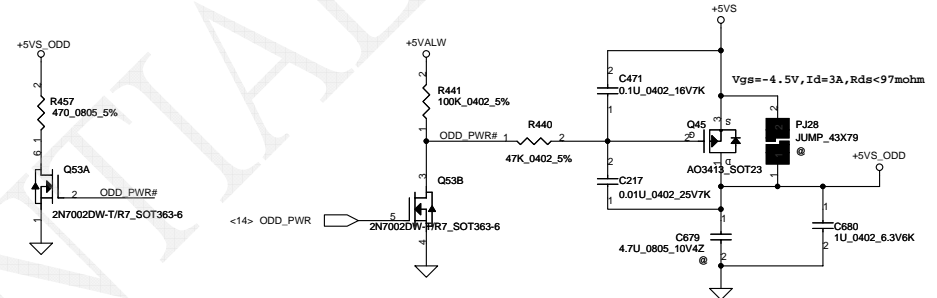
### +1.5V to +1.5VS



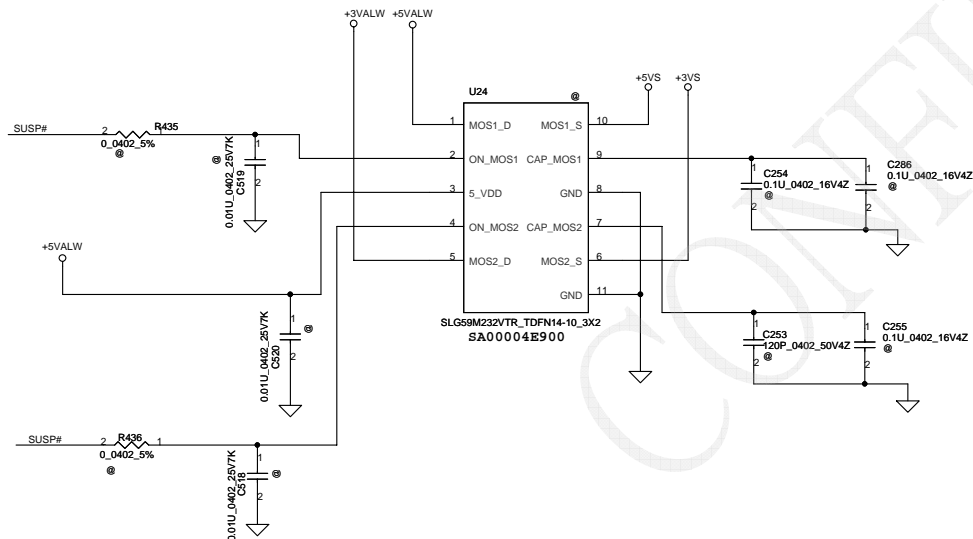
### +1.1VALW to +1.1VS



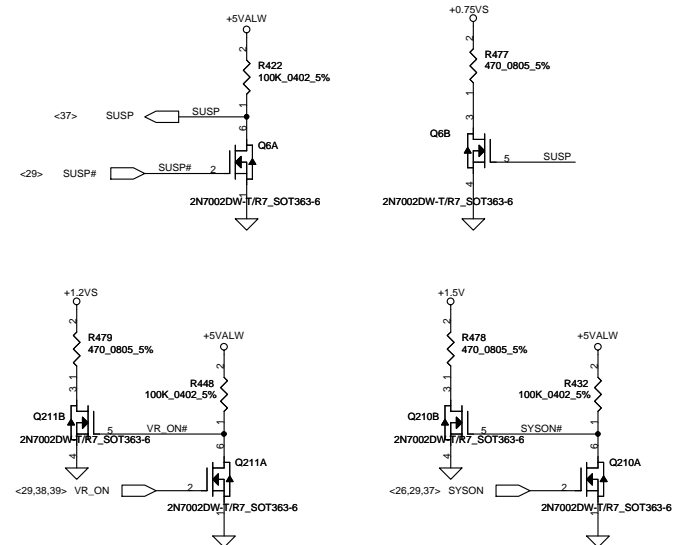
### +5VS TO +5VS\_ODD



Each 250pF on CAP\_MOS1 (2) will make Slew Rate(uS/V) increase of 100uS/V

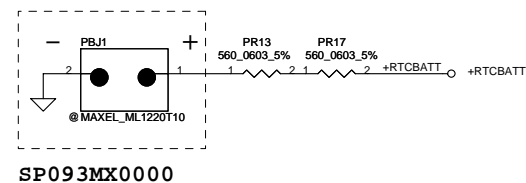
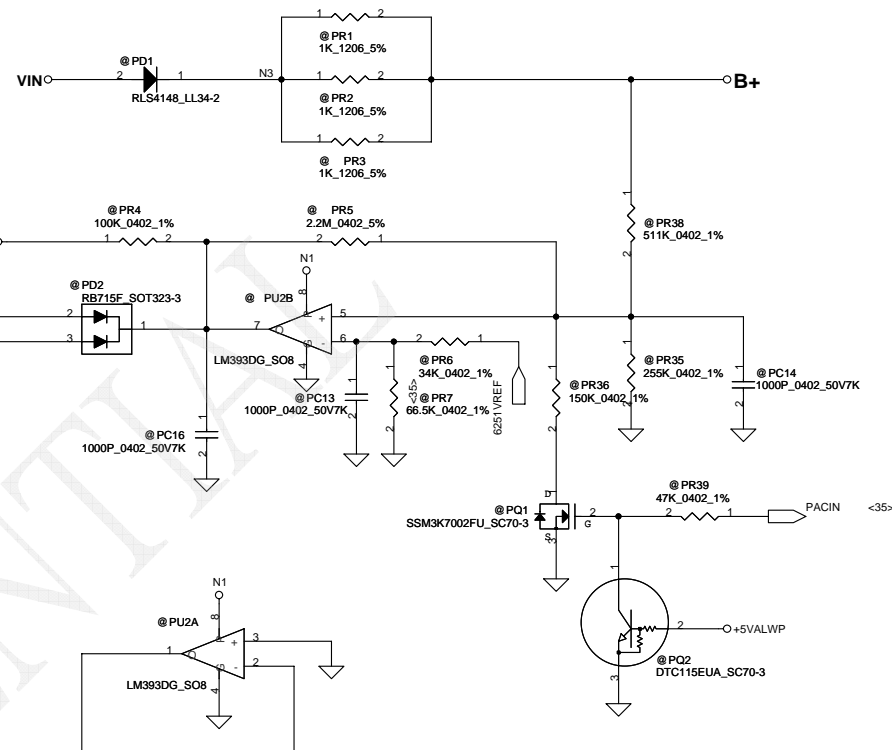
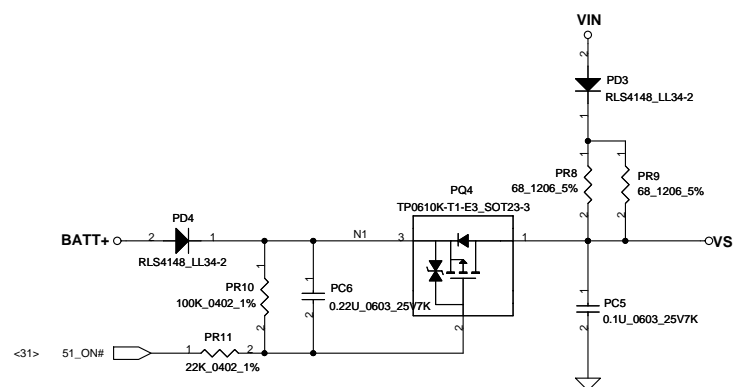


### Discharge

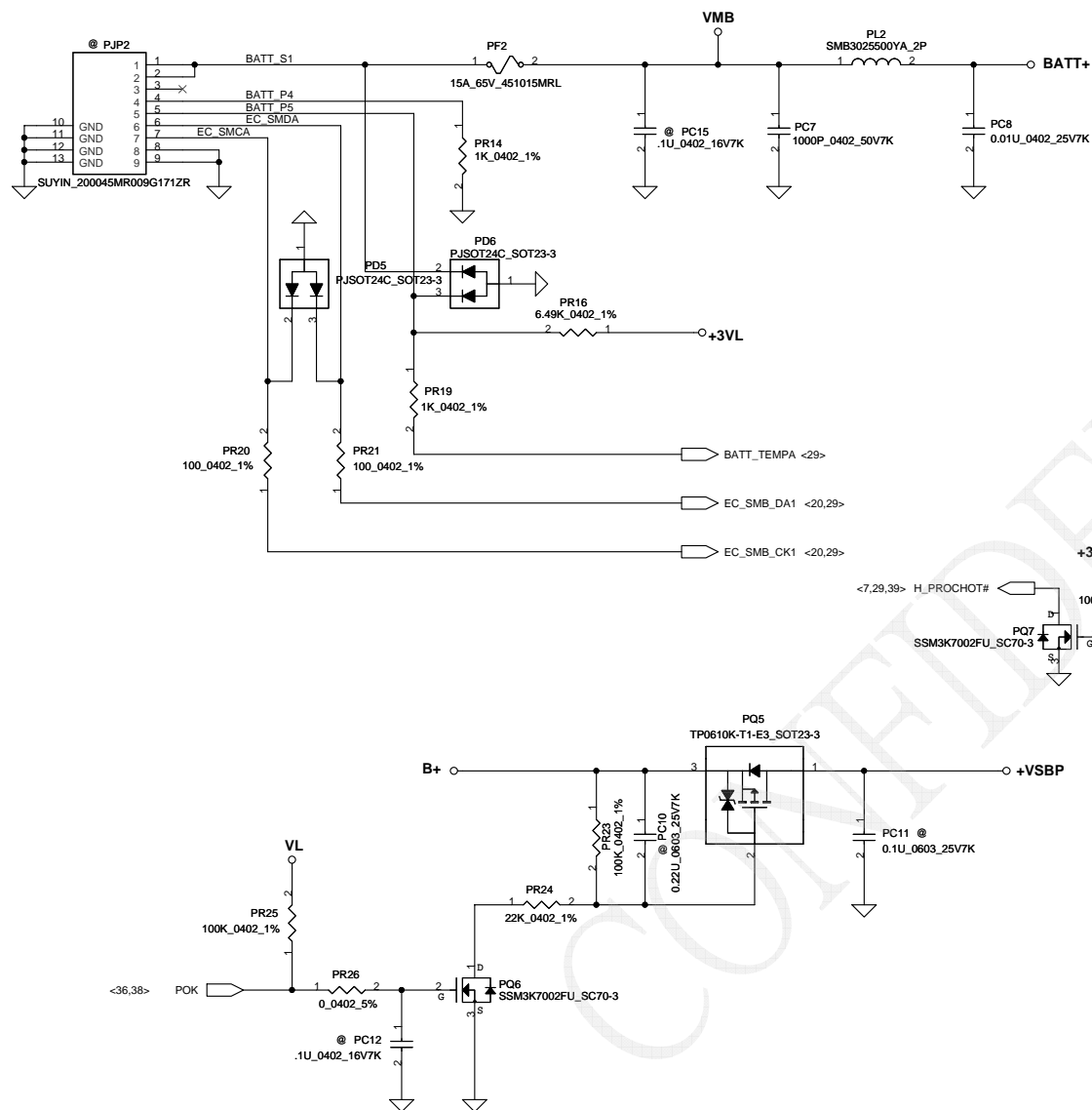


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PH1 under CPU bottom side :  
CPU thermal protection at 90 degree C  
Recovery at 56 degree C

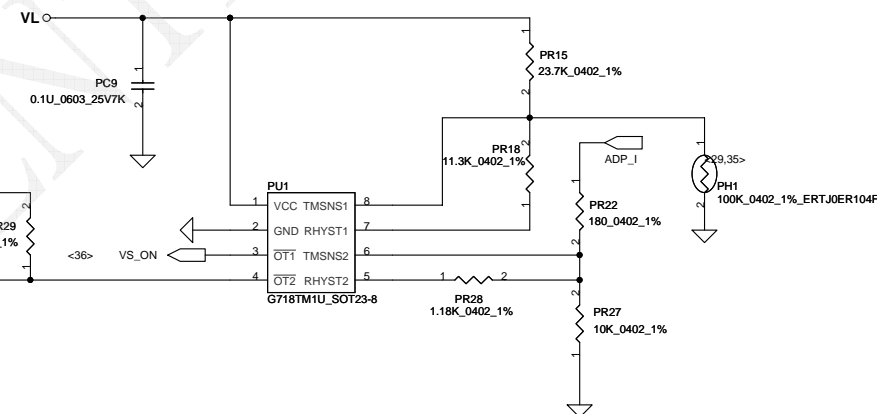
$$R_{set} = 3 * R_{tmh}$$

$$R_{hyst} = (R_{set} * R_{tml}) / (3 * R_{tml} - R_{set})$$

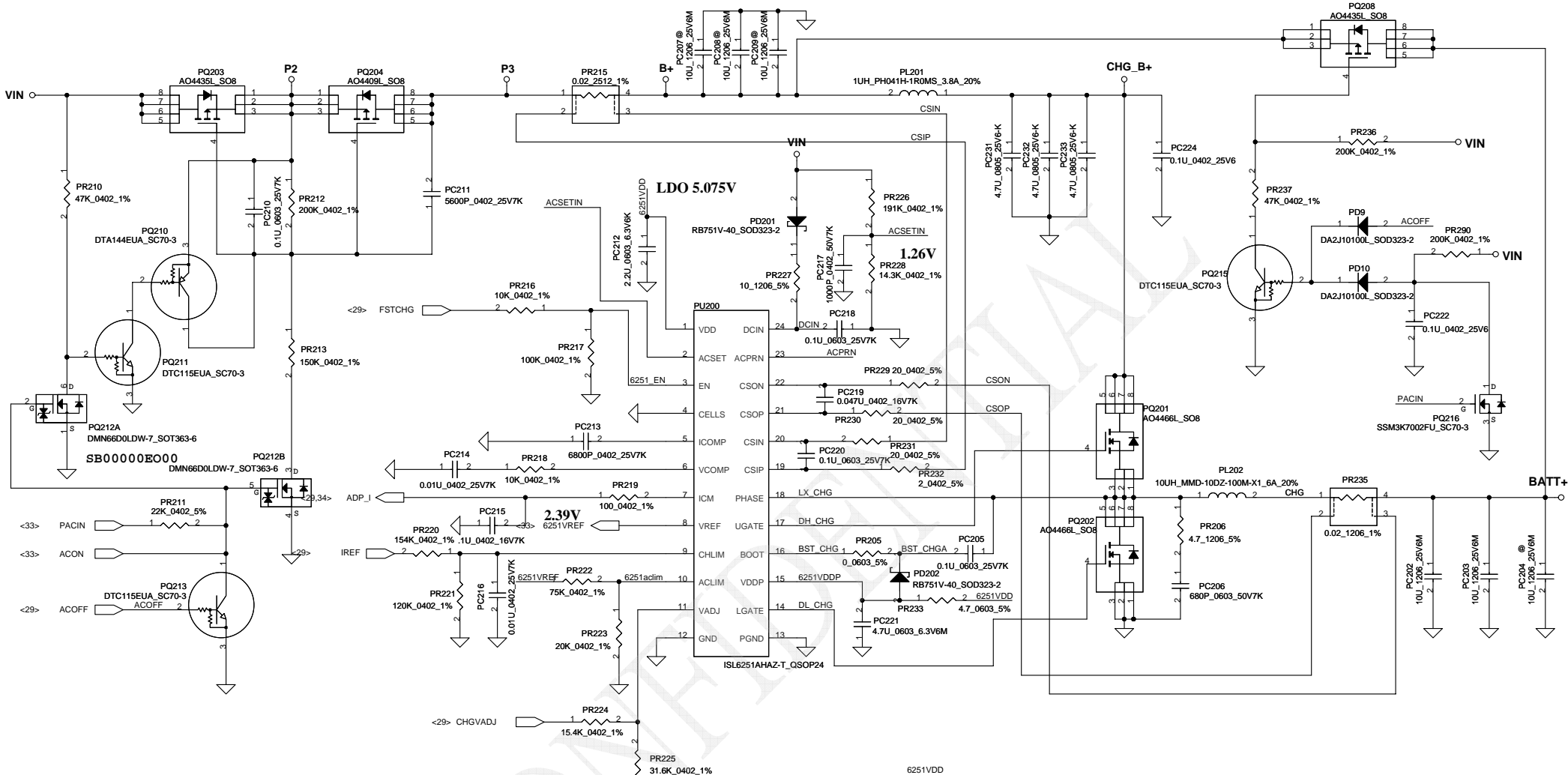
$$R_{tmh} \text{ at } 90C = 7.87K, R_{tml} \text{ at } 56C = 26.1K$$

$$R_{set} = 3 * 7.87K = 23.61K \Rightarrow 23.7K$$

$$R_{hyst} = (23.7K * 26.1K) / (3 * 26.1K - 23.7K) = 11.33K \Rightarrow 11.3K$$



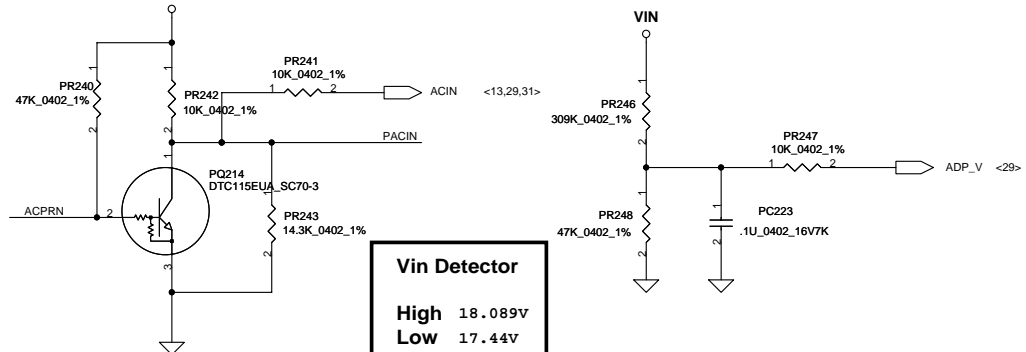
Adapter	CPSETIN	Throttle Watt	Recovery Watt	Throttle Point	Recovery Point
65W_UMA	no use	71.8W	62.45W	1.504V	1.308V



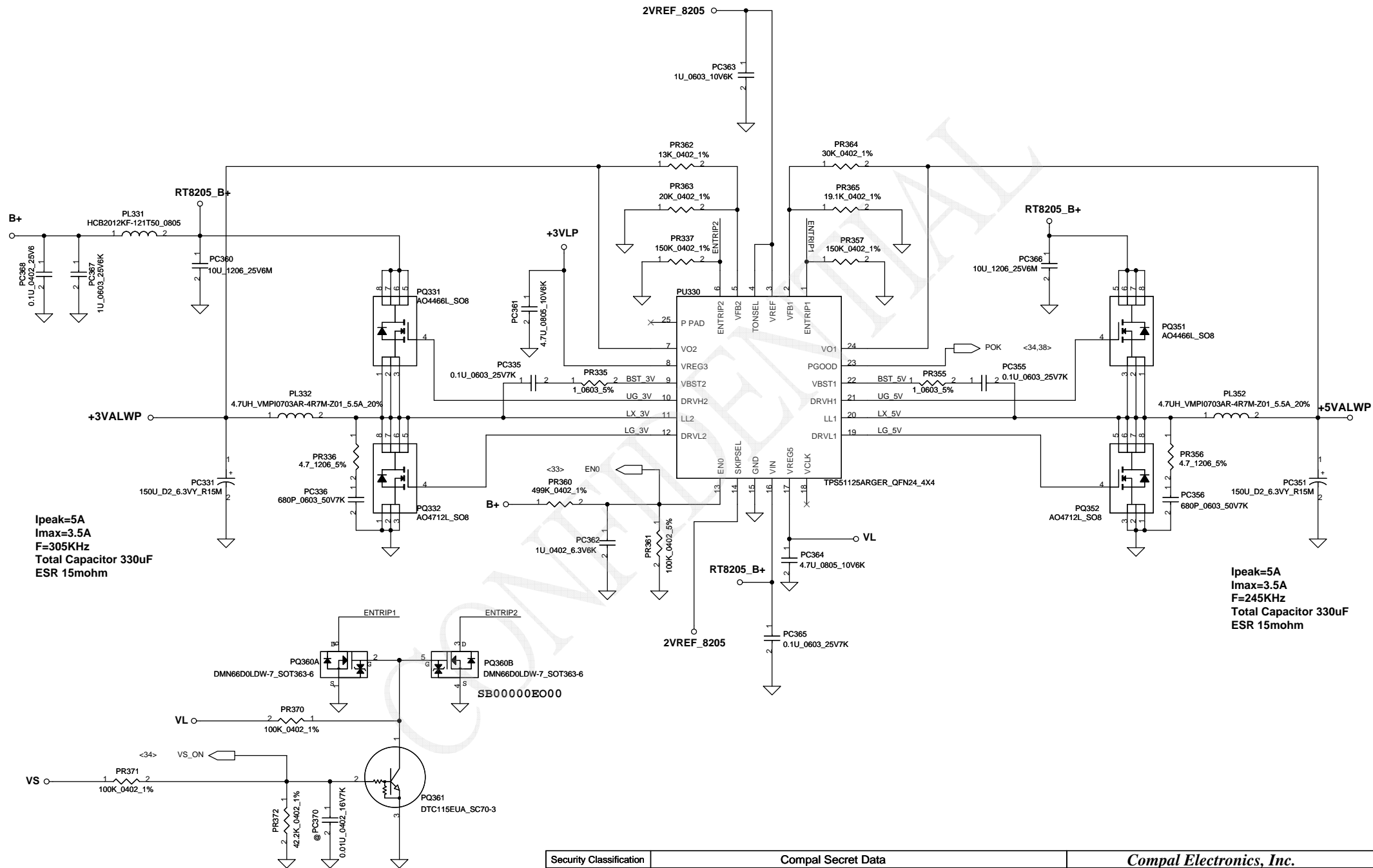
CC=0.25A~3.6A  
 IREF=0.9133\*Icharge  
 IREF=0.228V~3.288V  
 VCHLIM need over 88mV

Vcell	CHGVADJ
4V	0V
4.2V	1.889V
4.35V	3.30575V

CP mode CP= 92%\*Iada  
 UMA  
 Iada=0~3.947A(75W) CP=3.63A  
 Vaclim=1.1V(75W) PR222=24k, PR223=20k, PR215=0.02



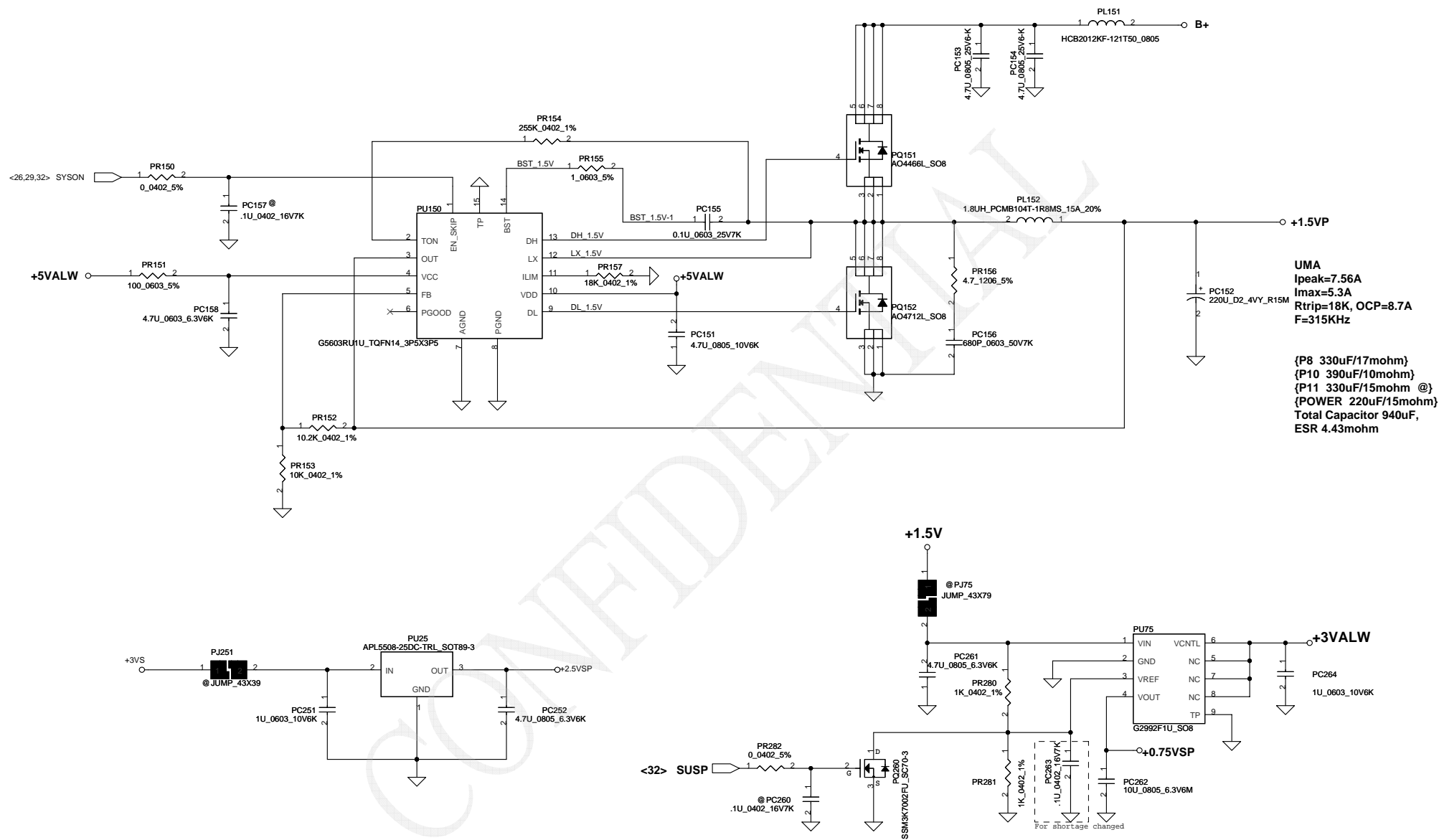
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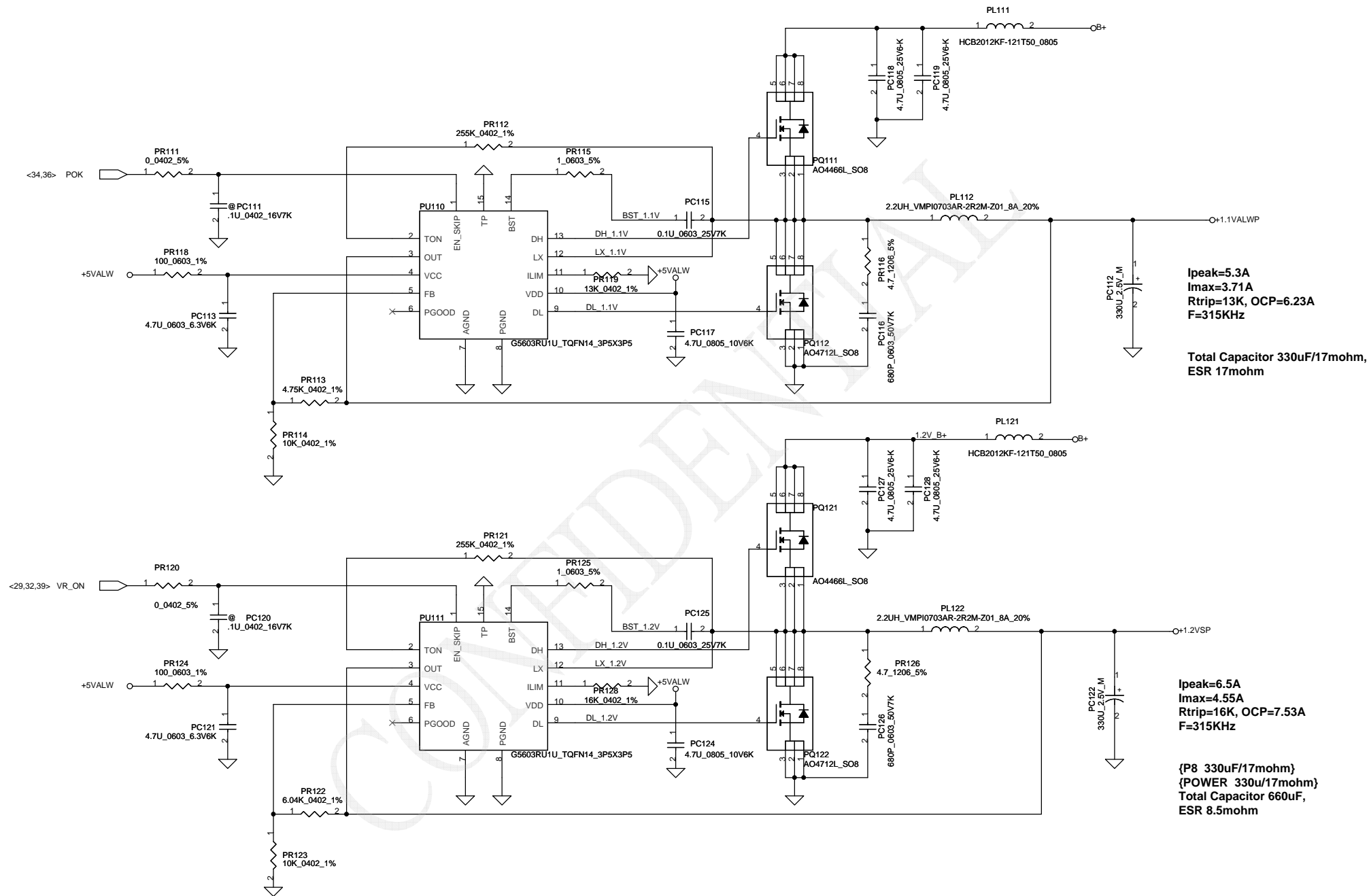
I<sub>peak</sub>=5A  
I<sub>max</sub>=3.5A  
F=305KHz  
Total Capacitor 330uF  
ESR 15mohm

I<sub>peak</sub>=5A  
I<sub>max</sub>=3.5A  
F=245KHz  
Total Capacitor 330uF  
ESR 15mohm

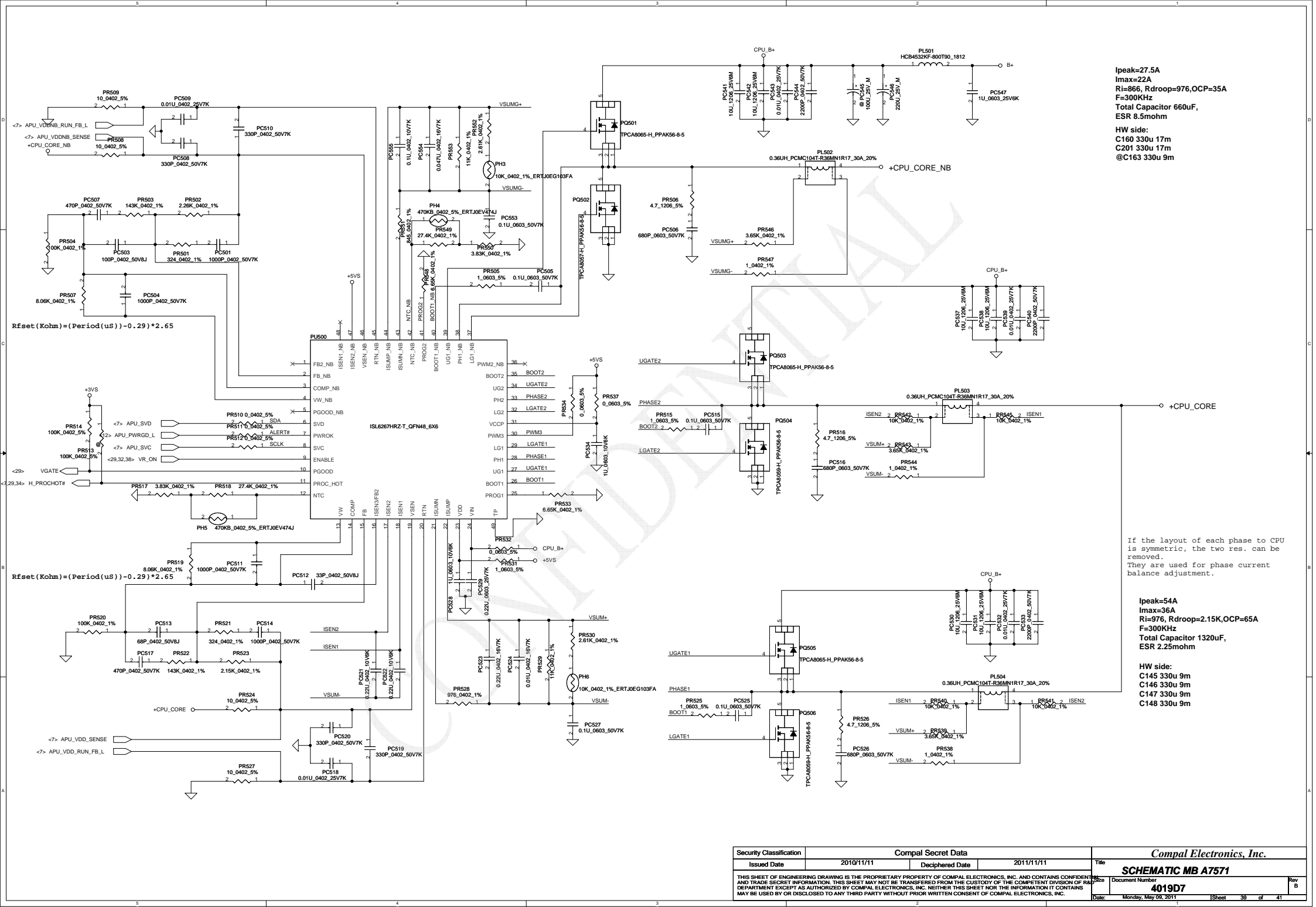
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Ipeak=27.5A  
Imax=22A  
Ri=866, Rdrrp=976, OCP=35A  
F=300KHz  
Total Capacitor 660uF,  
ESR 8.5mohm  
HW side:  
C160 330u 17m  
C201 330u 17m  
@C163 330u 9m

If the layout of each phase to CPU  
is symmetric, the two res. can be  
removed.  
They are used for phase current  
balance adjustment.

Ipeak=54A  
Imax=36A  
Ri=976, Rdrrp=2.15K, OCP=65A  
F=300KHz  
Total Capacitor 1320uF,  
ESR 2.25mohm  
HW side:  
C145 330u 9m  
C146 330u 9m  
C147 330u 9m  
C148 330u 9m

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# HW PIR (Product Improve Record)

QOQAE LA-7571P SCHEMATIC CHANGE LIST  
REVISION CHANGE: 0.2 TO 0.3

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	03/15	26	Add DT4	For ESD's request
2.	03/15	13	Delete ODD_PLUGIN#_FCH level shift since ODD has INT 1k PD	ODD has internal 1K PD
3.	03/15	25	Add level shift for CR_CPPE# leakage issue	For leakage issue
4.	03/15	13	Change HDMI_HPD to GEVENT10#	GEVENT9# has issue
5.	03/15	24	Change LOGO_LED to GPIO176 and WL_BT_LED to GPIO177	For LED flash issue
6.	03/17	25	Change RC16 from 22 ohm to 0 ohm for SDXC performance issue	For SDXC performance issue
7.	03/17	12	Change JCOMS to JCMOS	For naming rule
8.	03/17	07	Delete HDT signals	For ESD's request
9.	03/22	10	Add C21/C22/C23	For EMI's request
10.	03/22	31	Add C396/C397/C398/C399	For ESD's request
11.	03/22	21	Add C390 on +USB_VCCA	For ESD's request
12.	03/24	29	Delete net KS016 and KS017	W/O support 10 key
13.	03/24	07	Delete R127/R118/R119	For ESD's request
14.	03/24	31	Add C400/C40/C402	For ESD's request
15.	03/24	12	Add C332/C333	For ESD's request
16.	03/24	18	Add C287/C295	For ESD's request
17.	03/25	30	Change LPC debug port	For SW request
18.	03/28	18	Add C334	For ESD request
19.	03/28	12	Change C248 and C249 to 15PF	For RTC issue

REVISION CHANGE: 0.3 TO 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	04/26	16	Add C521,C342,C335 and C336	For EMI request
2.	04/26	16	Delete Q56 and add R371	No need for AMD A13
3.	04/26	31	Add C403 and C414	For EMI request
4.	04/26	31	Change SW2 and SW3 to 0	For Debug use
5.	04/27	08	Change C201 to 330/9mohm ))))))))	For Dynamic CPU_CORE_NB fail
6.	04/27	14	Delete 450 of U13	For Debug use
7.	04/27	10	Add C343/C344/C345/C346/C347/C348/C349/C350	For ESD request
8.	04/27	31	Add C426	For ESD request
9.	04/29	10	Change C343/C344/C345/C346/C347/C348/C349/C350 from 1u to 0.1u	For ESD request
10.	05/03	12)	Add C333 and C332	For ESD request
11.	05/03	13	Add C363	For ESD request